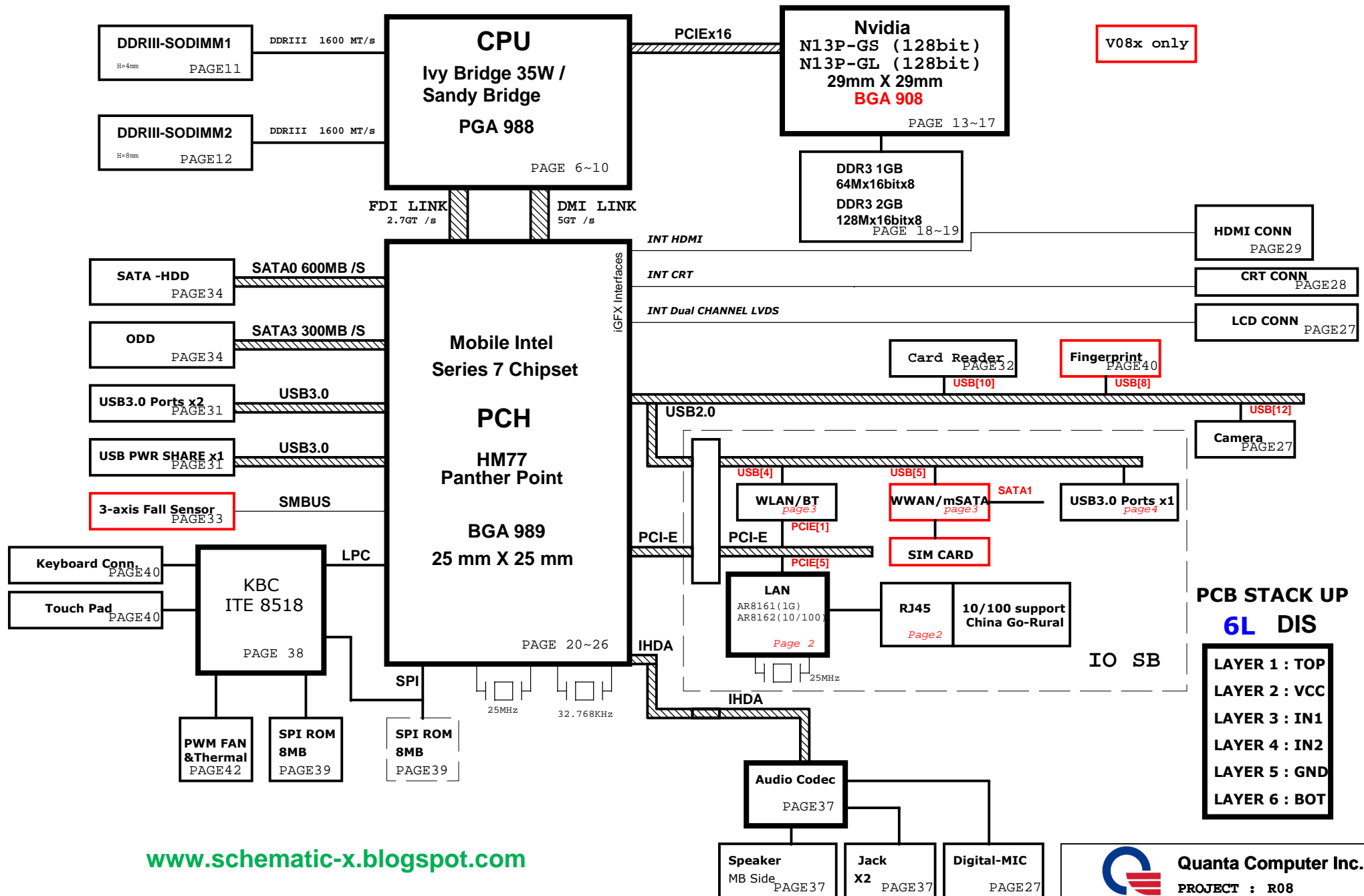
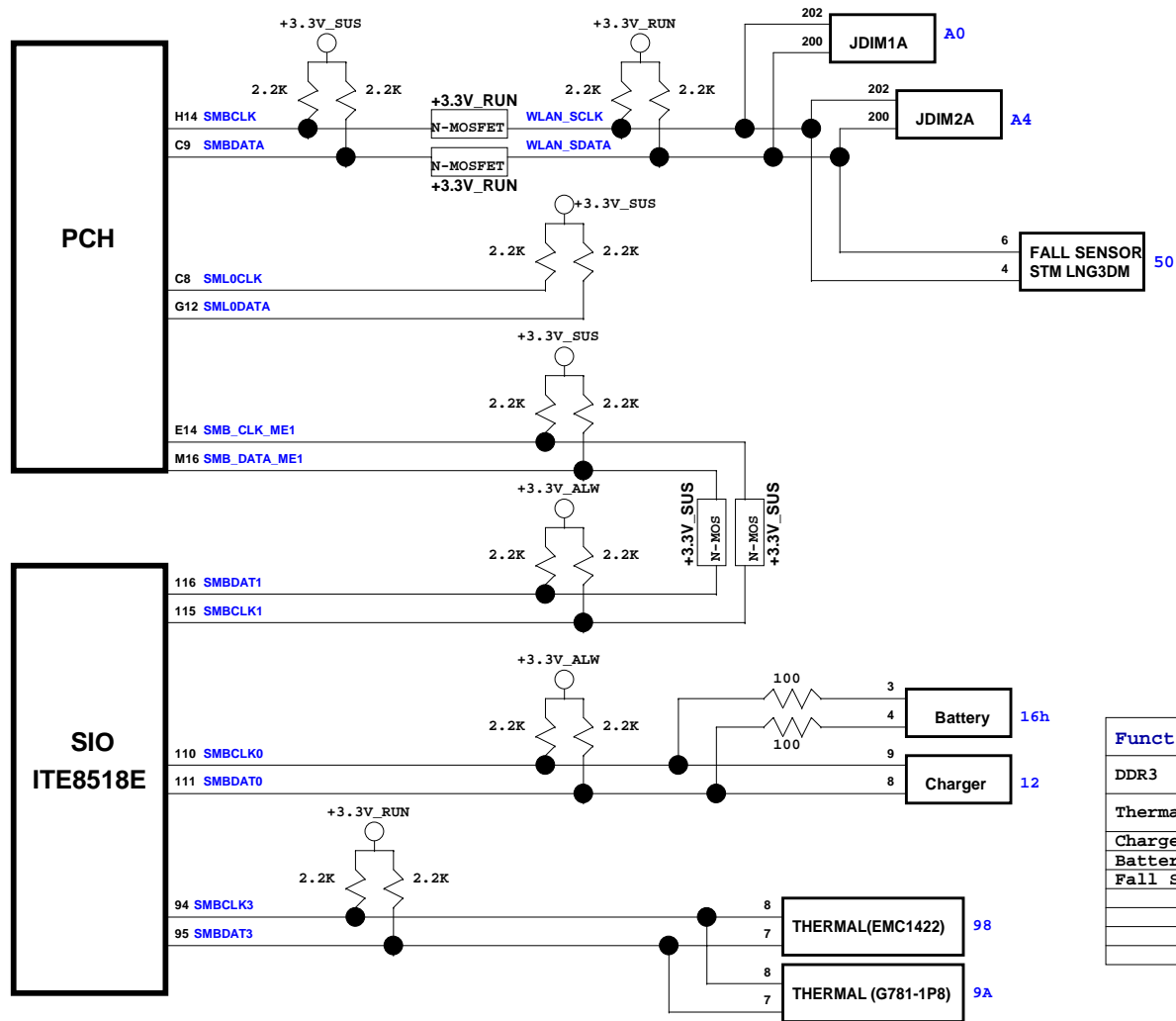


R08/V08 BLOCK DIAGRAM

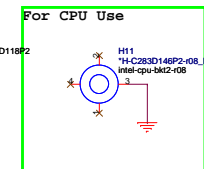
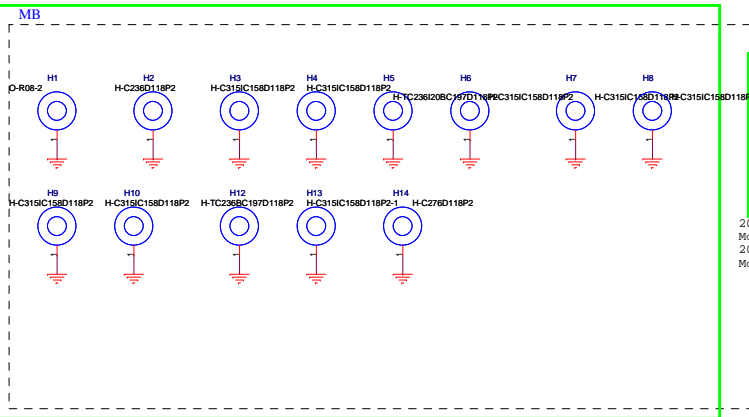
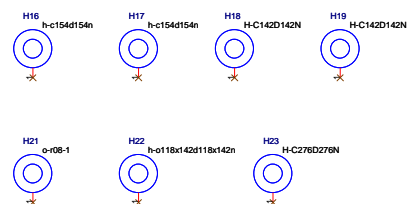


www.schematic-x.blogspot.com



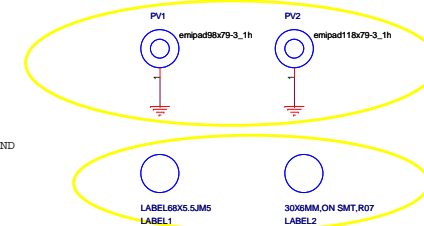
Function	IC	SMBus Address
DDR3	JDIM1A JDIM2A	A0h A4h
Thermal IC	EMC1422 G781-1P8	1001100xb (98h) 1001101xb (9Ah)
Charge IC	BQ24707ARGRR	0b0001001x (0x12h)
Battery	Battery	16h
Fall Sensor	STM LNG3DM	01010000 (50h)

SCREW PAD



20120206
Modify H11 pin1,2,3,4 no connect to GND
20120209
Modify H11 pin3 connect to GND

20120204
Modify PV1 PV2 subsystem ID to OTH

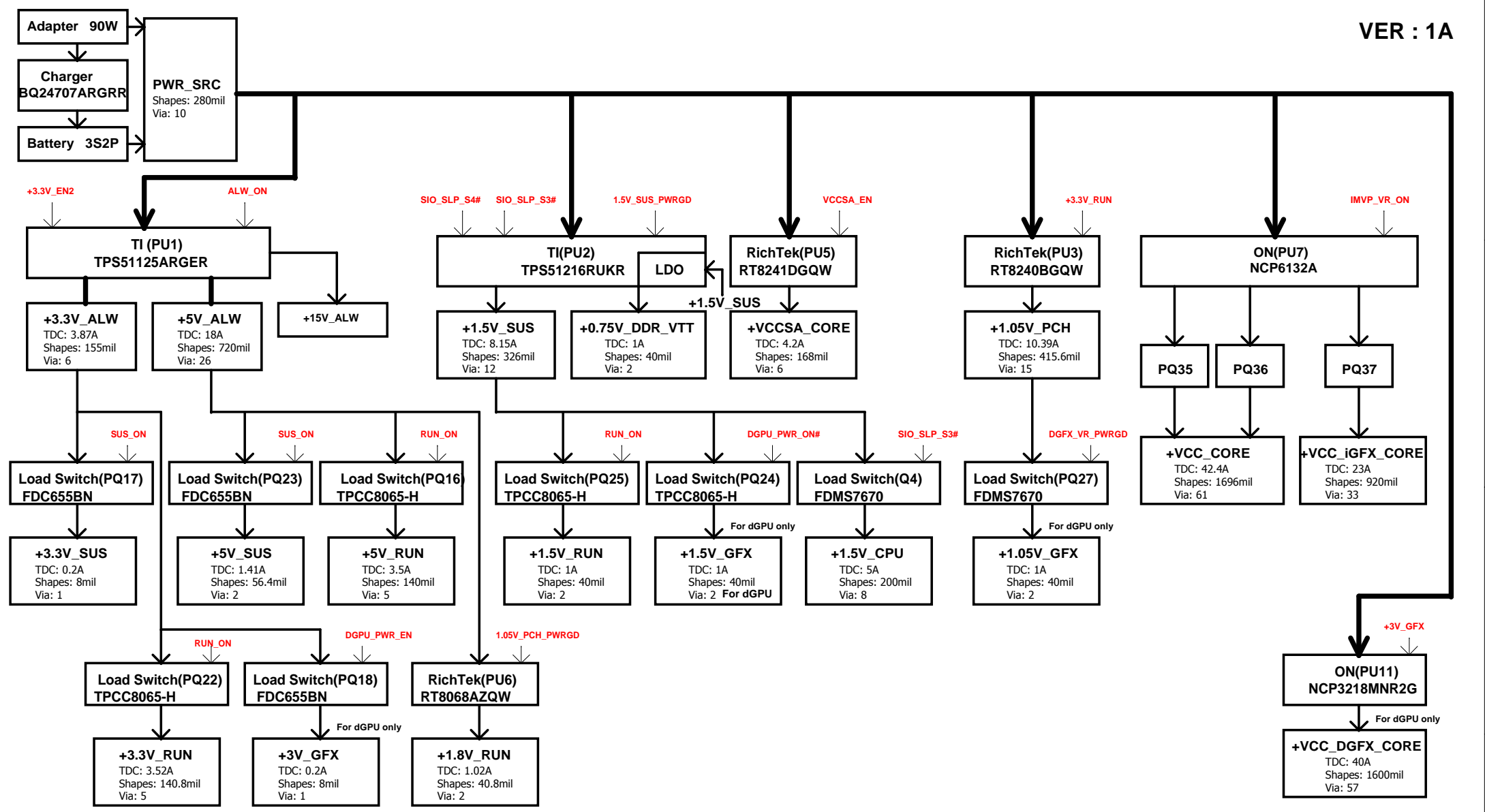


20120204
Add two label PV HCR07003010 and RCM5004013

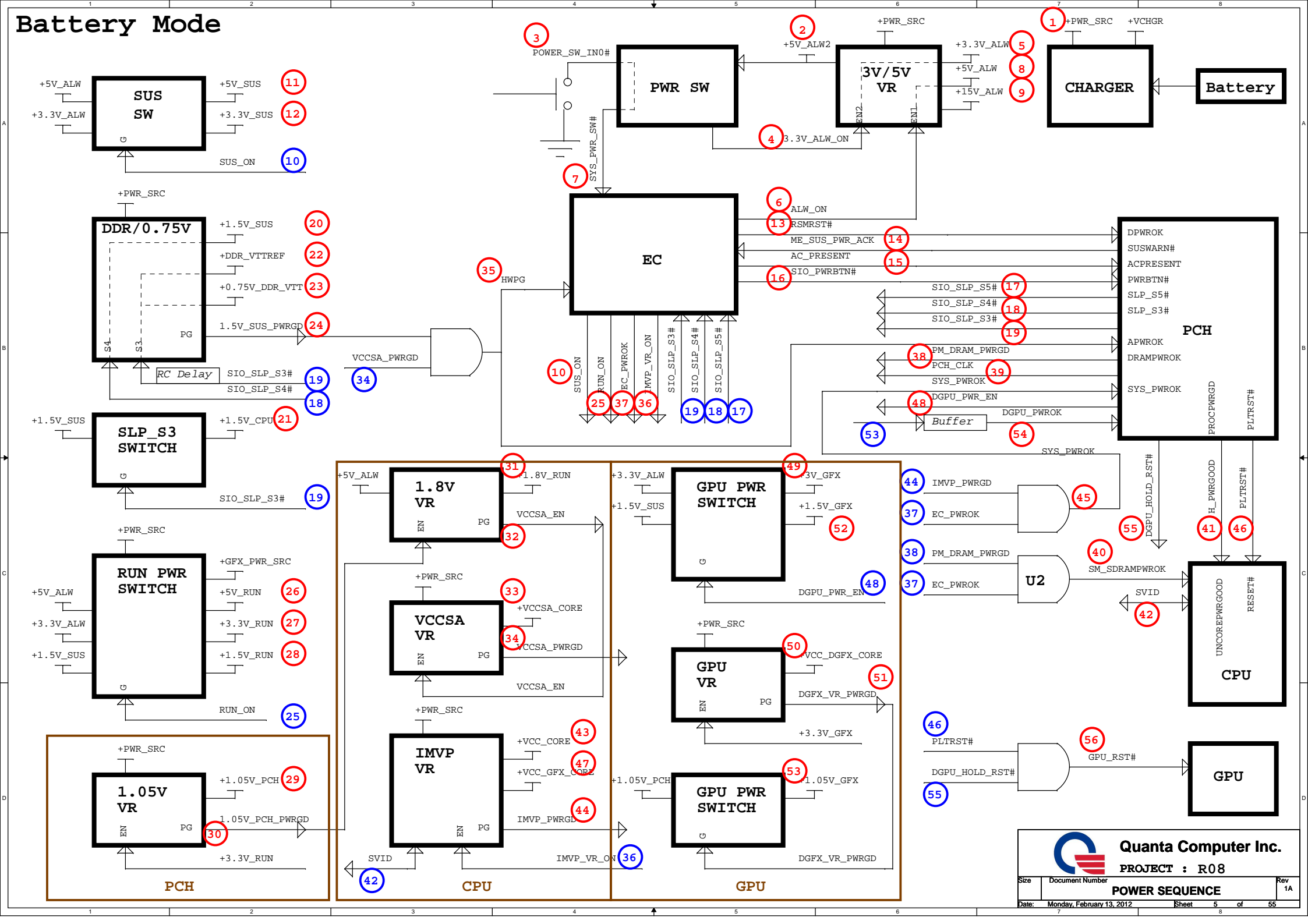
USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0/eSATA/ Power share/ debug port)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0)
USB4	MiniCard 1 (WLAN/BT)
USB5	MiniCard 2 (WWAN/WiMAX)
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	Touch panel (NC, for debug)
USB10	Card Reader
USB11	Express Card (NC)
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	ODD
SATA4	eSATA (NC)
SATA5	NC

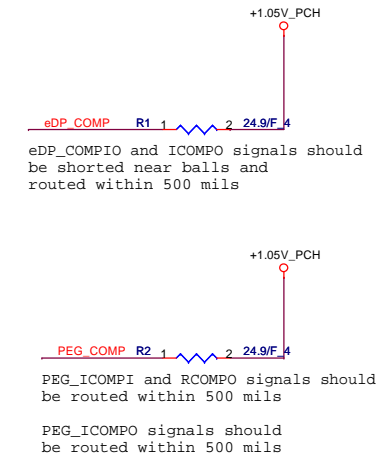
PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	WWAN (NC)
PCIE 3	Card reader (NC)
PCIE 4	NC
PCIE 5	LAN
PCIE 6	Express card (NC)
PCIE 7	NC
PCIE 8	NC



Battery Mode




DP & PEG Compensation

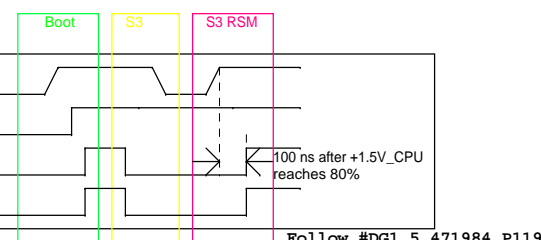
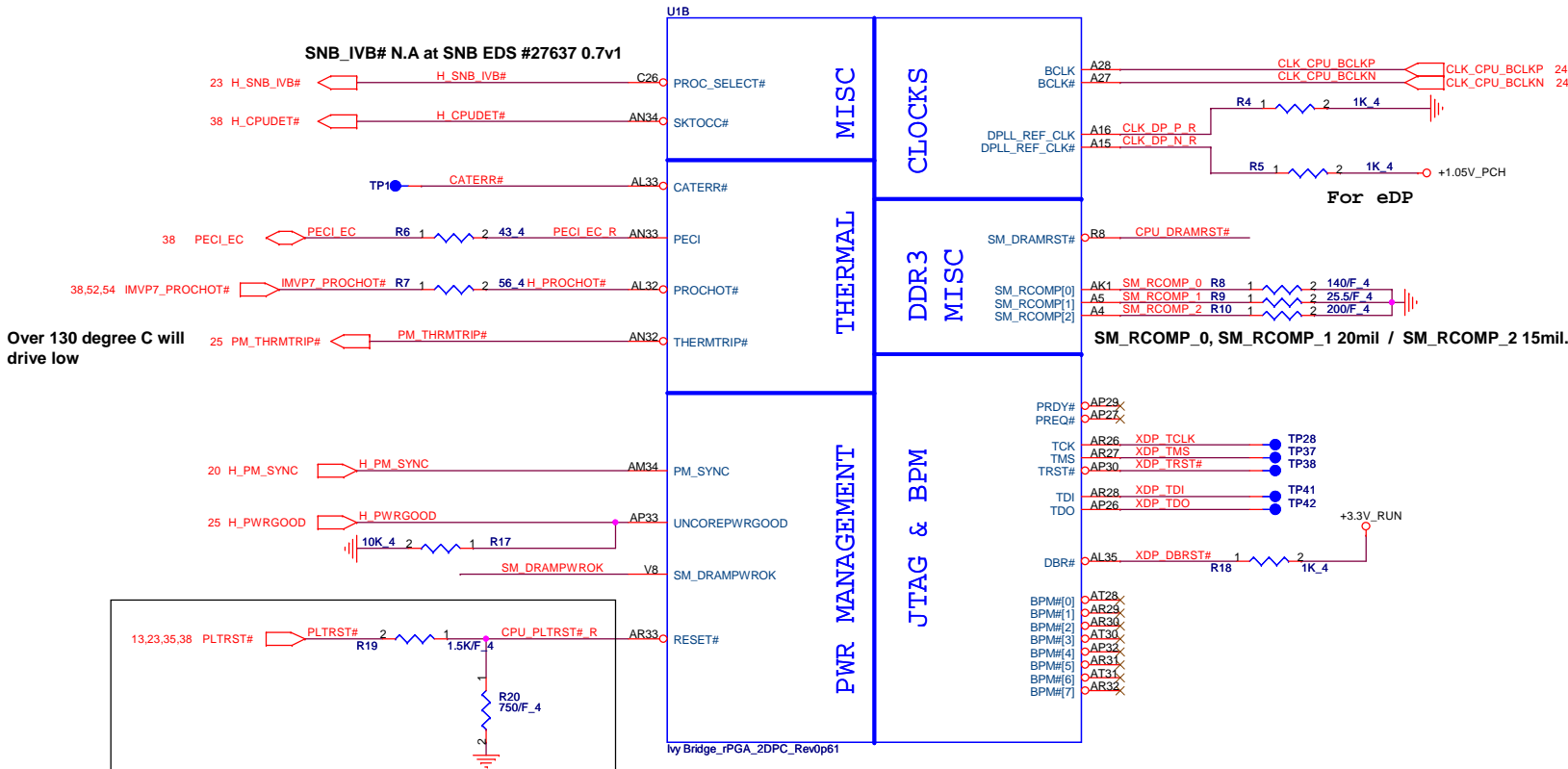


CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

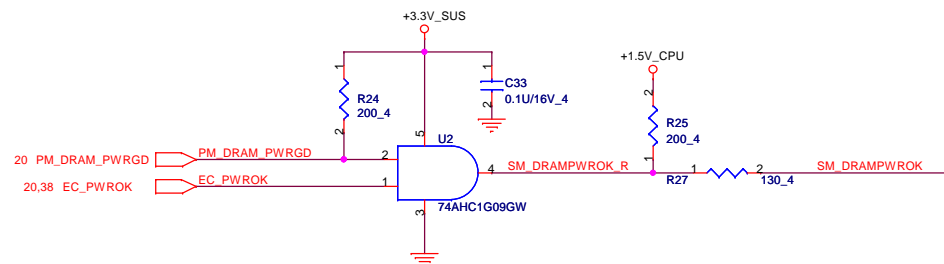
 Quanta Computer Inc. PROJECT : R08	
Size	Document Number
Ivy Bridge I/5	
Date: Monday, February 13, 2012	Sheet 6 of 55
	Rev 1A

Ivy Bridge Processor (CLK,MISC,JTAG)



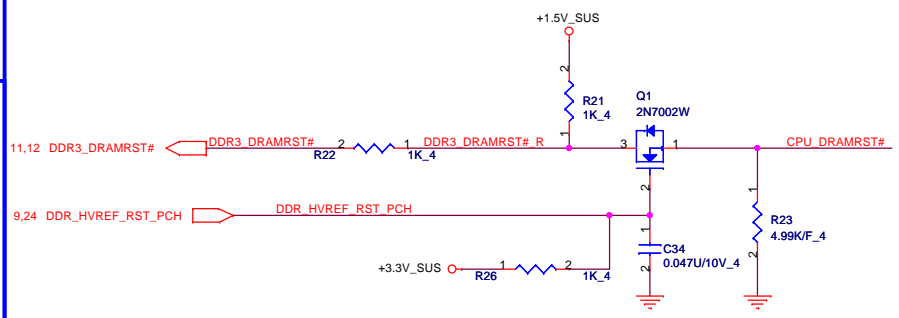
Follow #DG1.5 471984 P128

DDR Power Gating Topology

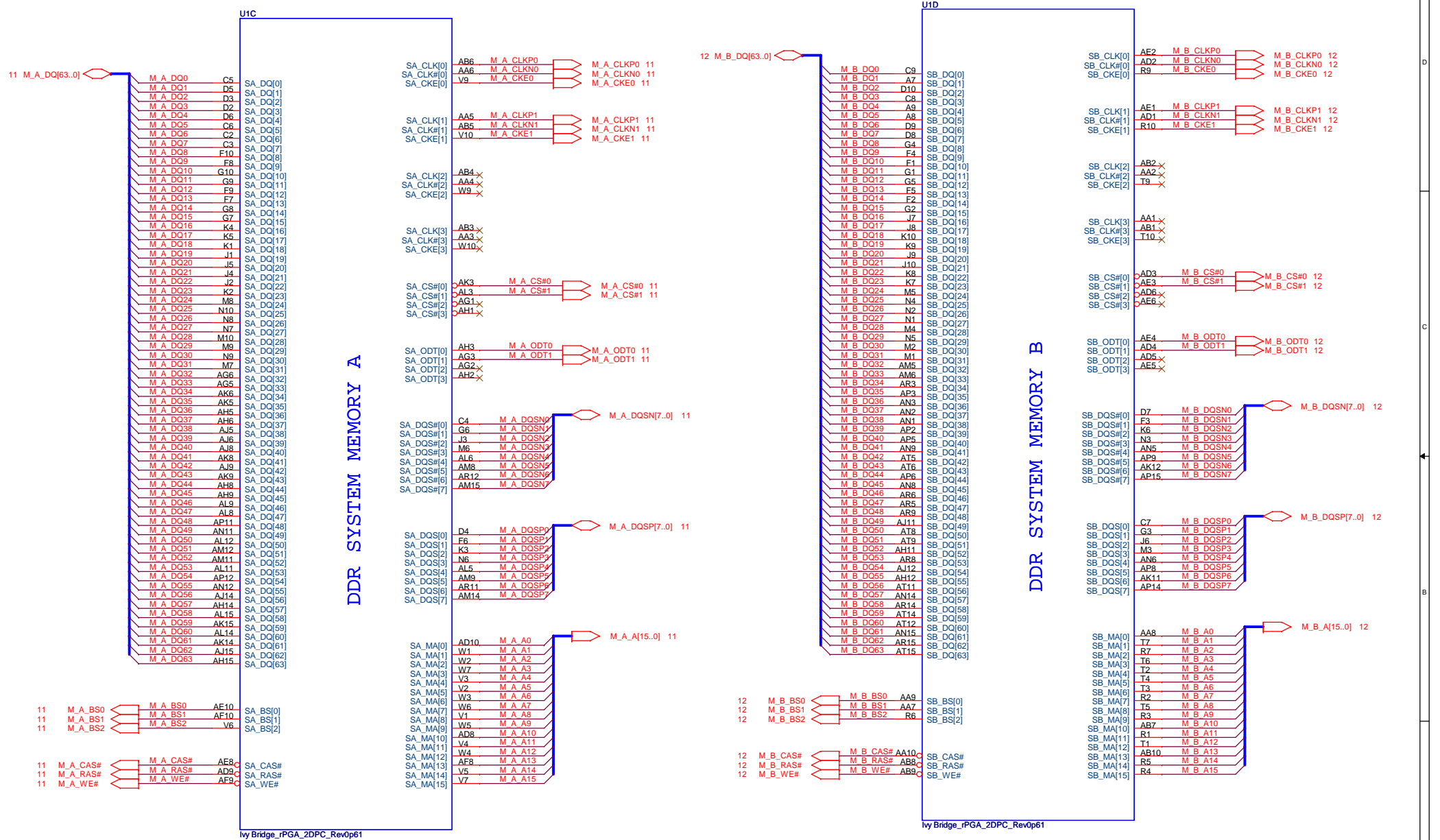


Follow #DG1.5 471984 P130

DRAMRST# Routing Illustration



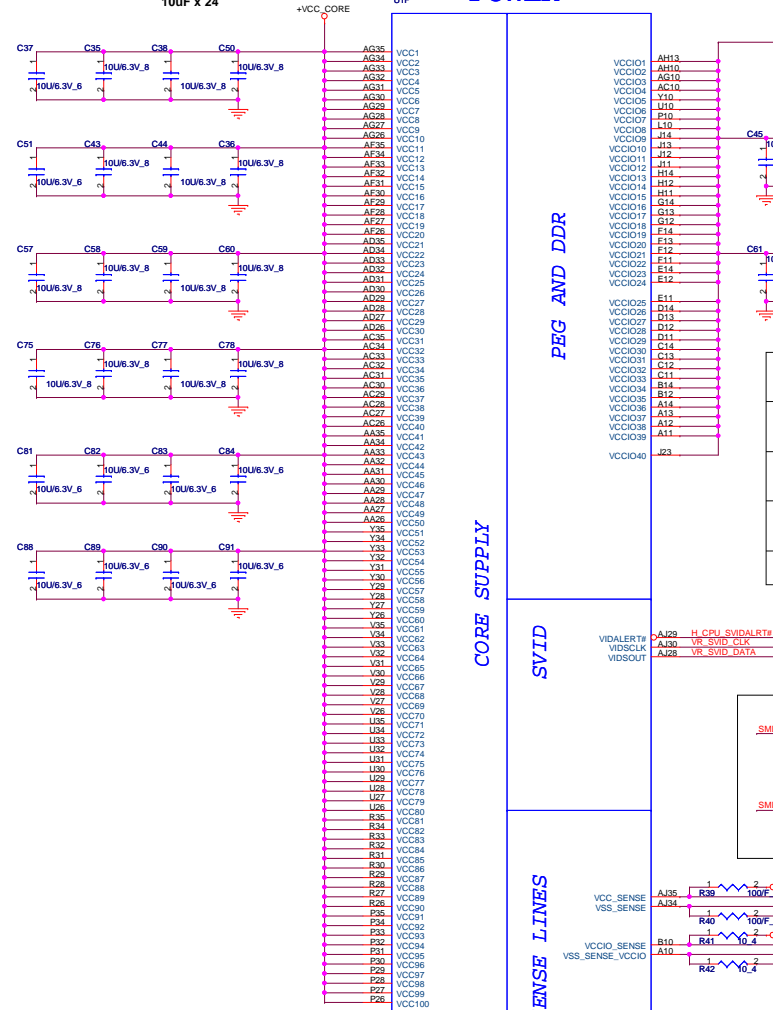
Ivy Bridge Processor (DDR3)



Ivy Bridge Processor (GRAPHIC POWER)

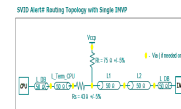
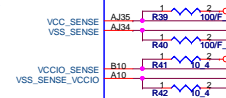
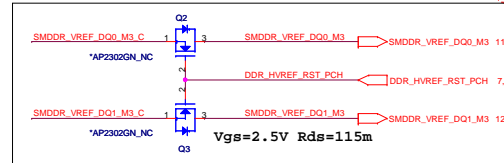
CPU VGT
SNB: 21.5A
IVY: 33A
10uF x 12

POWER



Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	27-33Ω	<25 mils
VCCA_XG_SENSE / VSSA_XG_SENSE	100Ω		
VCCIO_SENSE / VSS_SENSE_VCCIO	10Ω	55Ω	
VCCSA	100Ω		

M3 VREF



Layout note: need routing together and ALERT needs to be between CLK and DATA

SVID CLK



- Place PU resistor close to CPU

SVID DATA

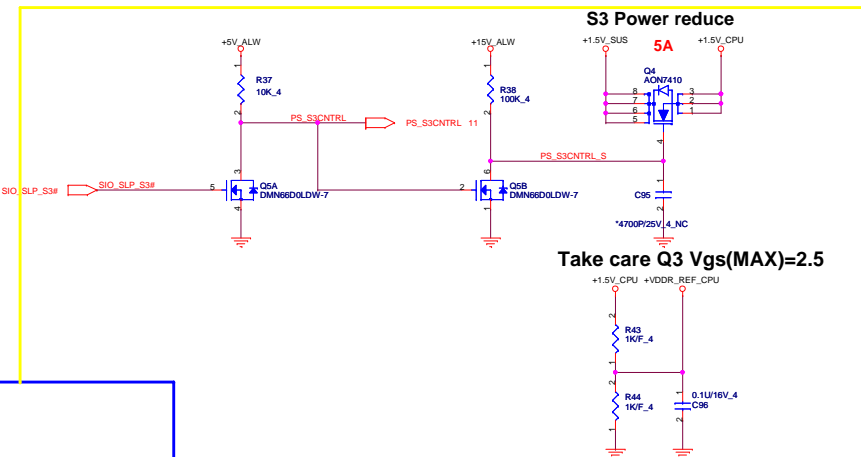


Place PU resistor close to CPU

SVID ALERT



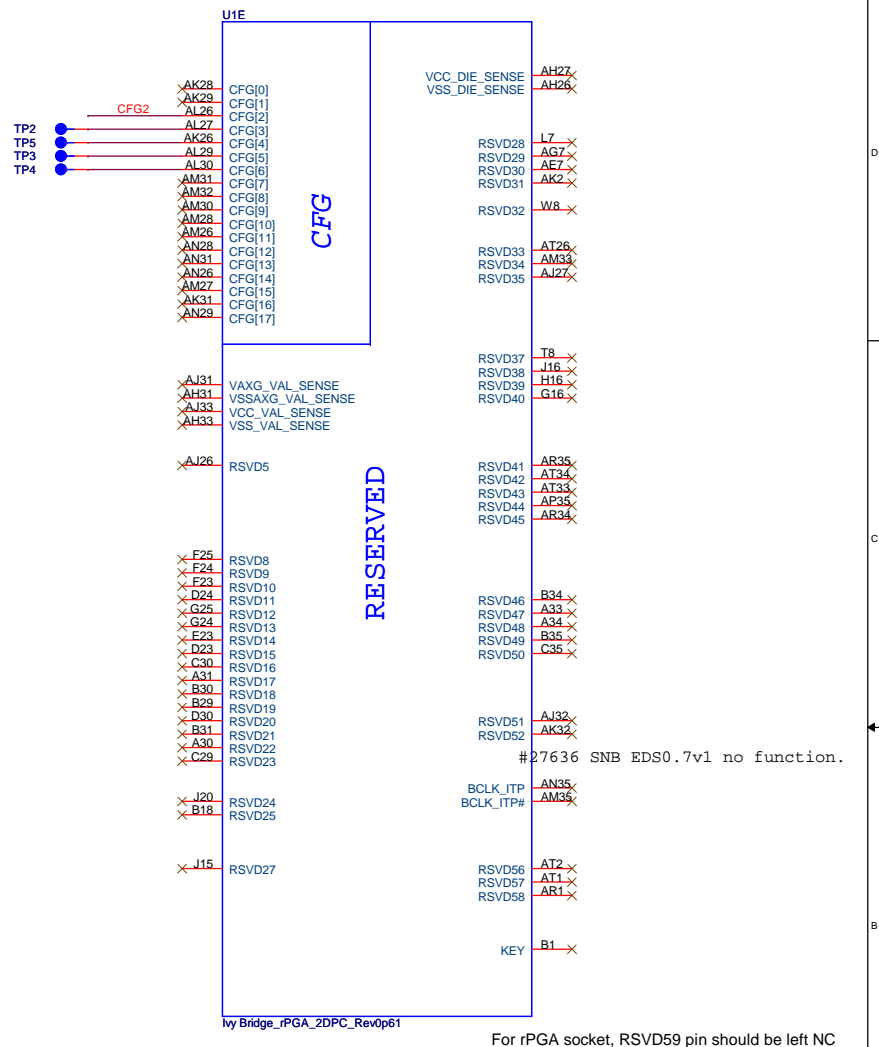
20,38,48 SIO_SLP_S3# SIO_SLP

**Quanta Computer Inc.**

PROJECT :R08

Size	Document Number	Rev
	Ivy Bridge 4/5	1A
Date:	Monday, February 13, 2012	Sheet 9 of 55

Ivy Bridge Processor (RESERVED, CFG)



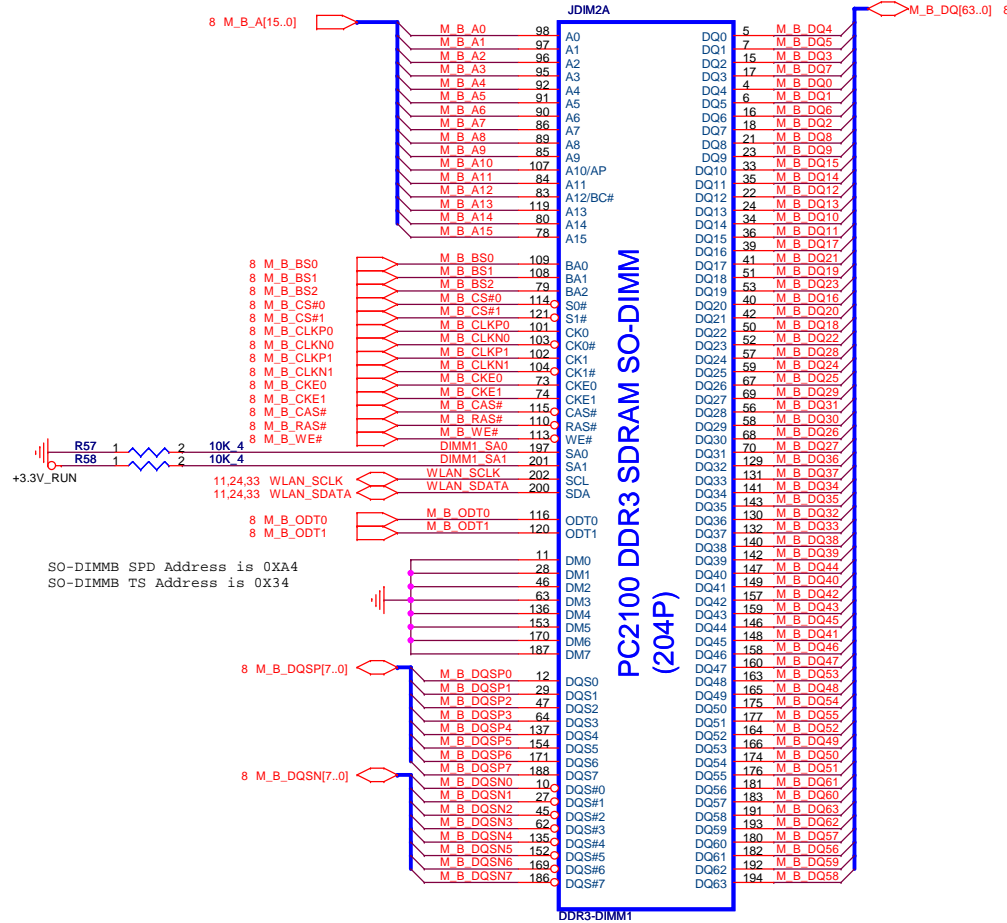
```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

The CFG signals have a default value of '1' if not terminated on the board.

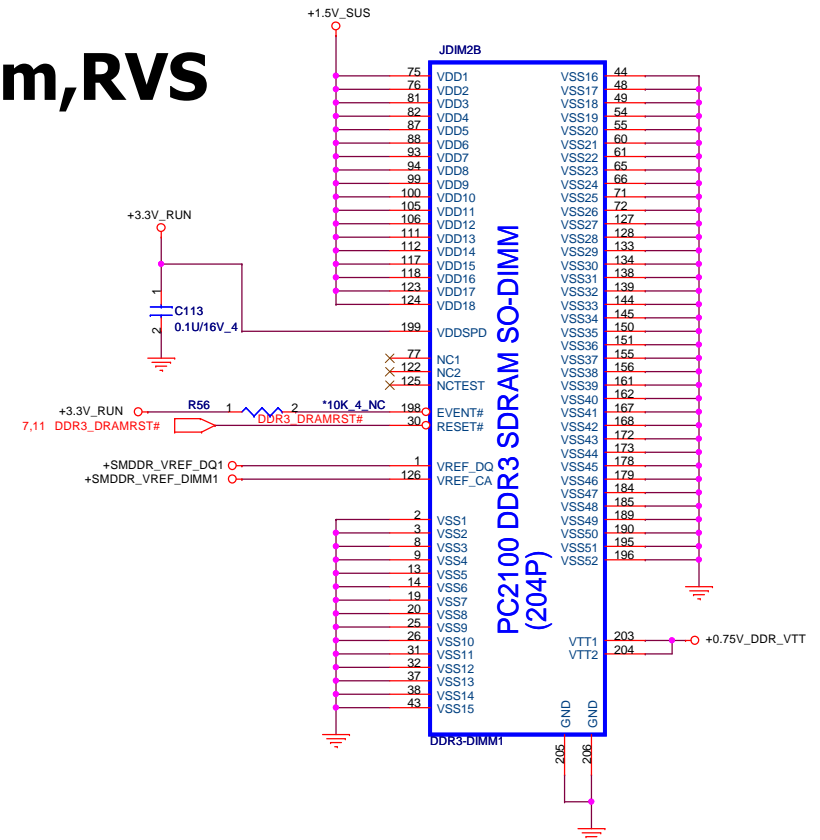


Date: Monday, February 13, 2012 Sheet 10 of 55

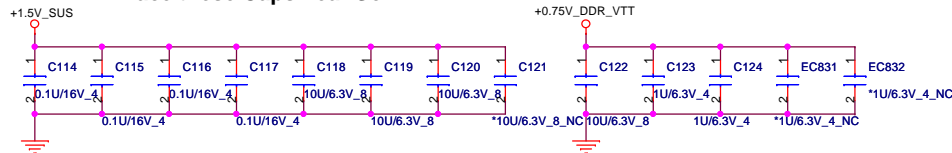
H=4mm,RVS



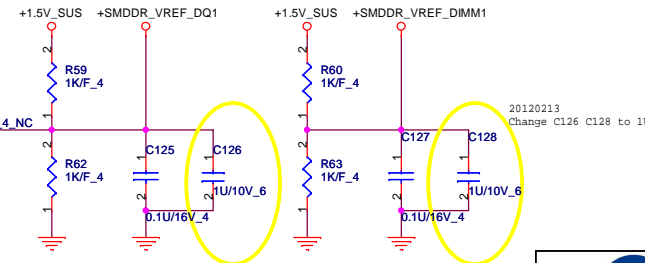
PC2100 DDR3 SDRAM SO-DIMM (204P)



Place these Caps near So-Dimm1.



M1 VREF

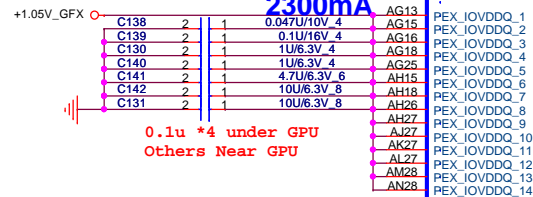


Quanta Computer Inc.

PROJECT : R08

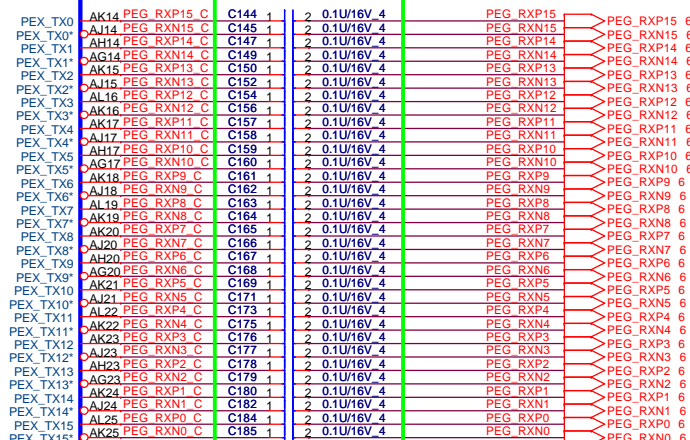
Change U3 to AJ0N13P0T49(WINCON)

REX 101



+1.05V_GFX

C186 1 2 *0.1U/16V 4 NC
C187 1 2 *0.1U/16V 4 NC
C188 1 2 0.1U/16V 4

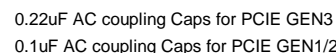


PEX_TSTCLK_OUT
 PEX_TSTCLK_OUT#
 PEX_RST#
 PEX_CLKREQ#
 PEX_TERM
 TESTMODE

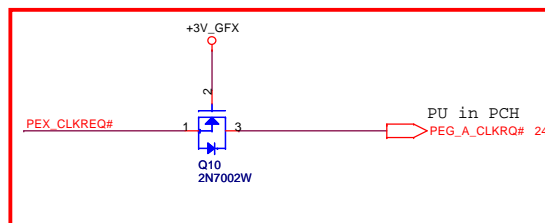
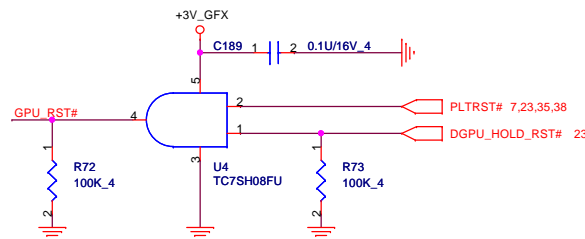
AJ26 PEX_TSTCLK#
 AJ12 GPU_RST#
 AK12 PEX_CLKREQ#
 AP29 PEX_TERM
 AK11 TESTMODE

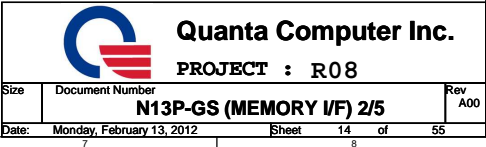
R68 2 1 *200_4_NC
 R69 2 1 10K_4
 R70 1 2 2.49K/4
 R71 1 2 10K_4

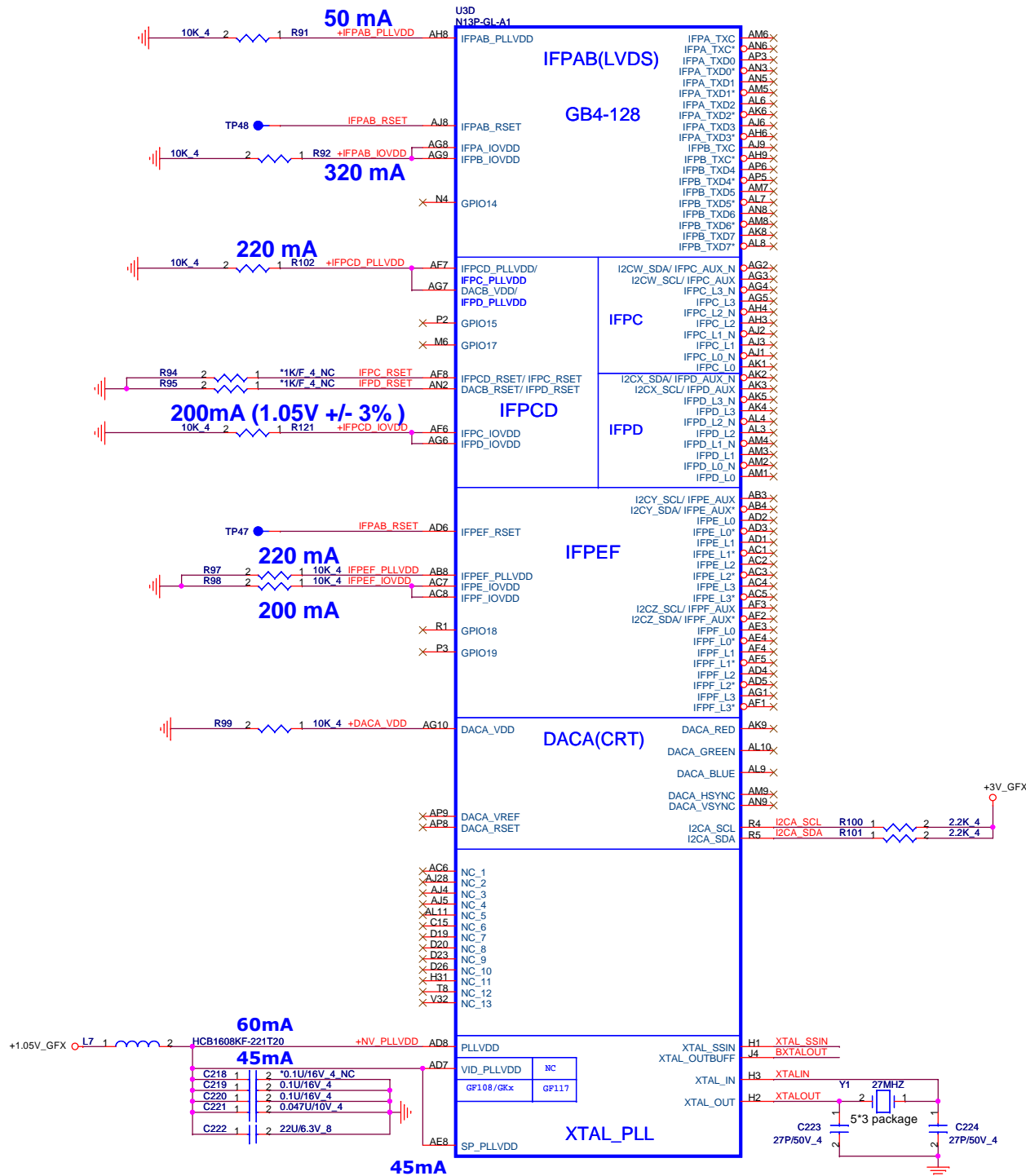
+3V_GFX



0101 0100 00 0000/101_1(ENHANCED)

[illegible]





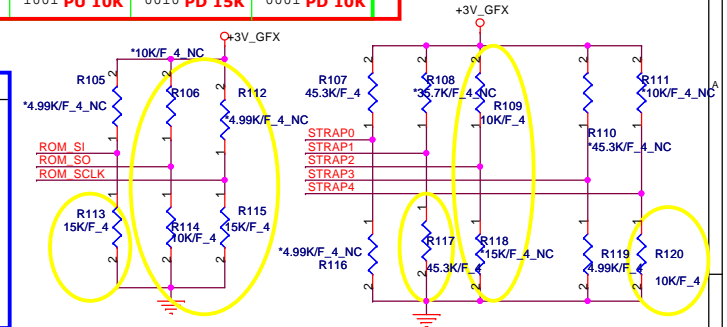
10 kΩ pull-down only if no spread chip used.

N13P-GL (AJ0N13P0T02)
N13P-GS for Turbo (AJ001070T00)

Strap Bit	Description
USER[3:0]	1111 EDID is used
3GIO_PADCFG [3:0]	0110 Notebook Default
PCI_DEVID[5:0]	D2 PCI Device ID
SORx_EXPOSED [3:0]	0000 Audio capability on each display port Not in use
DP_PLL_VDD33V	1 Default
PCIE_MAX_SPEED	1 PCIE Gen2/3 capable
PCI_SPEED_CHANGE_GEN3	0 Default
RAMCFG[3:0]	0010 Default Hynix1G
PCIE_PLL_TERMINATION	0 PCIE PLL termination disable (Default)
PEX_PLL_EN_TERM	0 No video BIOS ROM
SUB_VENDOR	01 Frame Buffer size Reserve
FB[1:0]	0 Default (1GPU)
SMB_ALT_ADDR	0 Default (1GPU)
VGA_DEVICE	1 Default (non 3D)

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

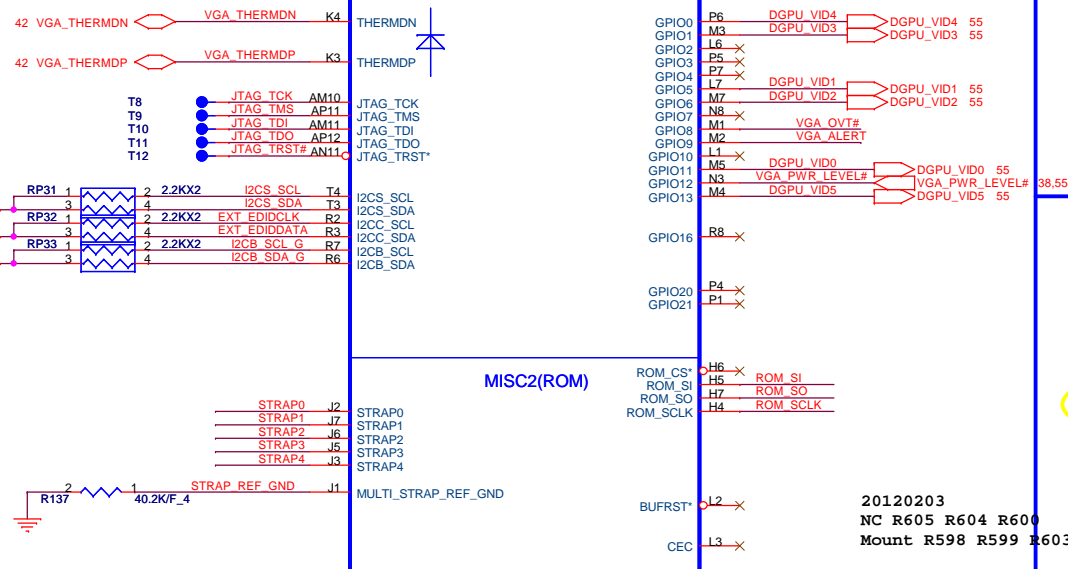


10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1% (0402)]
24.9K/F 4: CS32492FB16 [RES CHIP 24.9K 1/16W +1% (0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0010
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0001
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1001
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0111
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

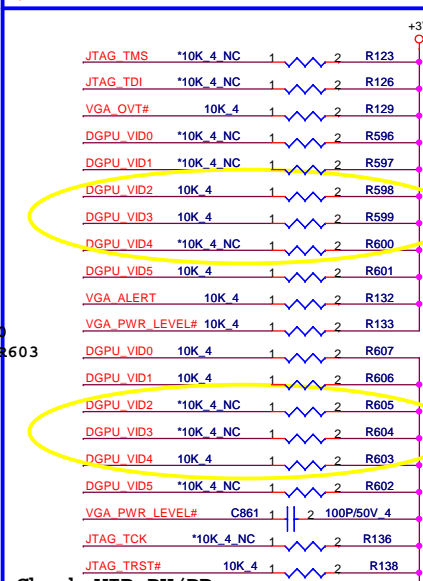
Default: Hynix VRAM 2G (0110) VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0000	Reserve	Reserved	Reserve	Reserve	PD 5K
0001	Reserve	Reserved	Reserve	Reserve	PD 10K
0010	DDR3 64Mx16, 900MHz	Hynix	AKD5LZWTW07	H5T1G63DFR-11C	PD 15K
0011	DDR3 64Mx16, 900MHz (G-die)	Samsung	AKD5EGGT509	K4W1G1646G-BC11	PD 20K
0110	DDR3 128Mx16, 900MHz	Hynix	AKD5MGWTW06	H5T1Q638FR-11C	PD 35K
0111	DDR3 128Mx16, 900MHz	Samsung	AKD5MGWT507	K4W2G1646C-HC11	PD 45K



20120203
NC R605 R604 R600
Mount R598 R599 R603

	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GL	0.95V	0	0	1	1	0	1
N13P-GS	0.9V	0	0	0	0	1	1



GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	NVDD_VID4
1	IN	N/A	NVDD_VID3
2	OUT	HIGH	NC
3	OUT	HIGH	NC
4	OUT	HIGH	NC
5	OUT	N/A	NVDD_VID1
6	OUT	N/A	NVDD_VID2
7	OUT	N/A	NC
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	NC
11	OUT	N/A	NVDD_VID0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	NVDD_VID5

GPIO ASSIGNMENTS



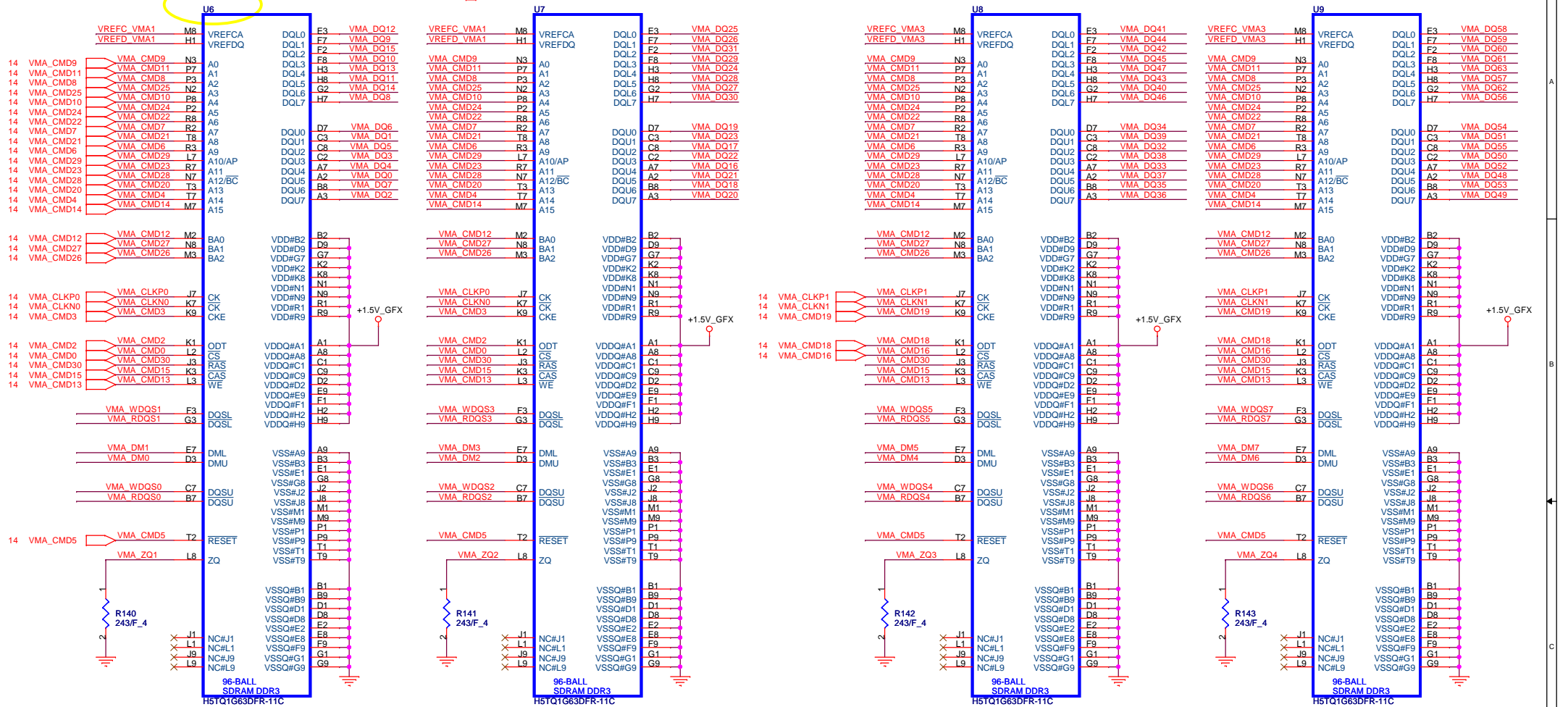
Quanta Computer Inc.

PROJECT : R08

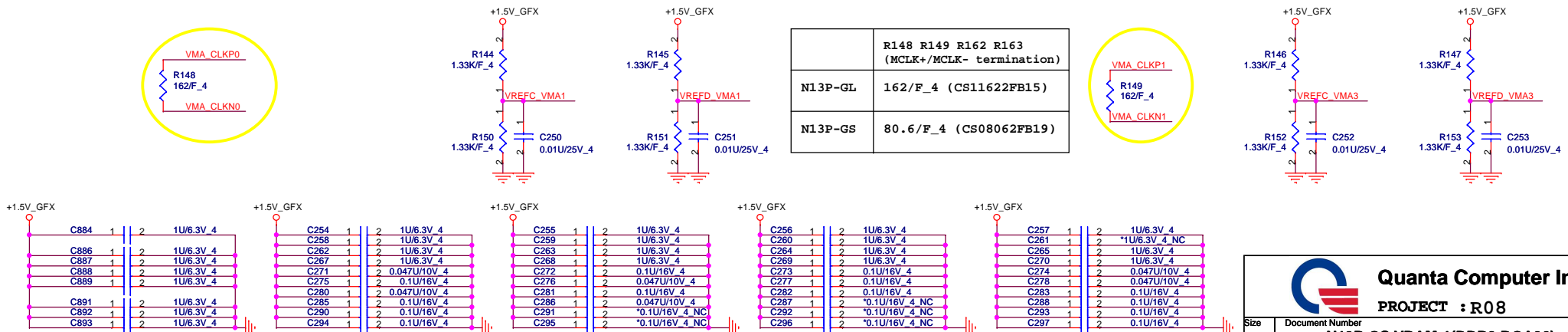
Size	Document Number	Rev
	N13P-GS (GPIO&STRAPS) 4/5	A00
Date:	Monday, February 13, 2012	Sheet 16 of 55

Change U6~U13 to AKD5LZWTW07 (hynix 1G)

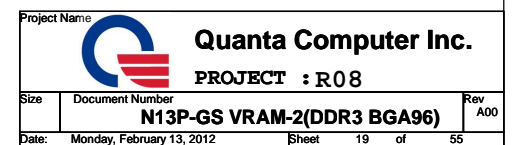
```
14 VMA_DQ[63..0]  •
14 VMA_DM[7..0]   •
14 VMA_WDQS[7..0] •
14 VMA_RDQS[7..0] •
```



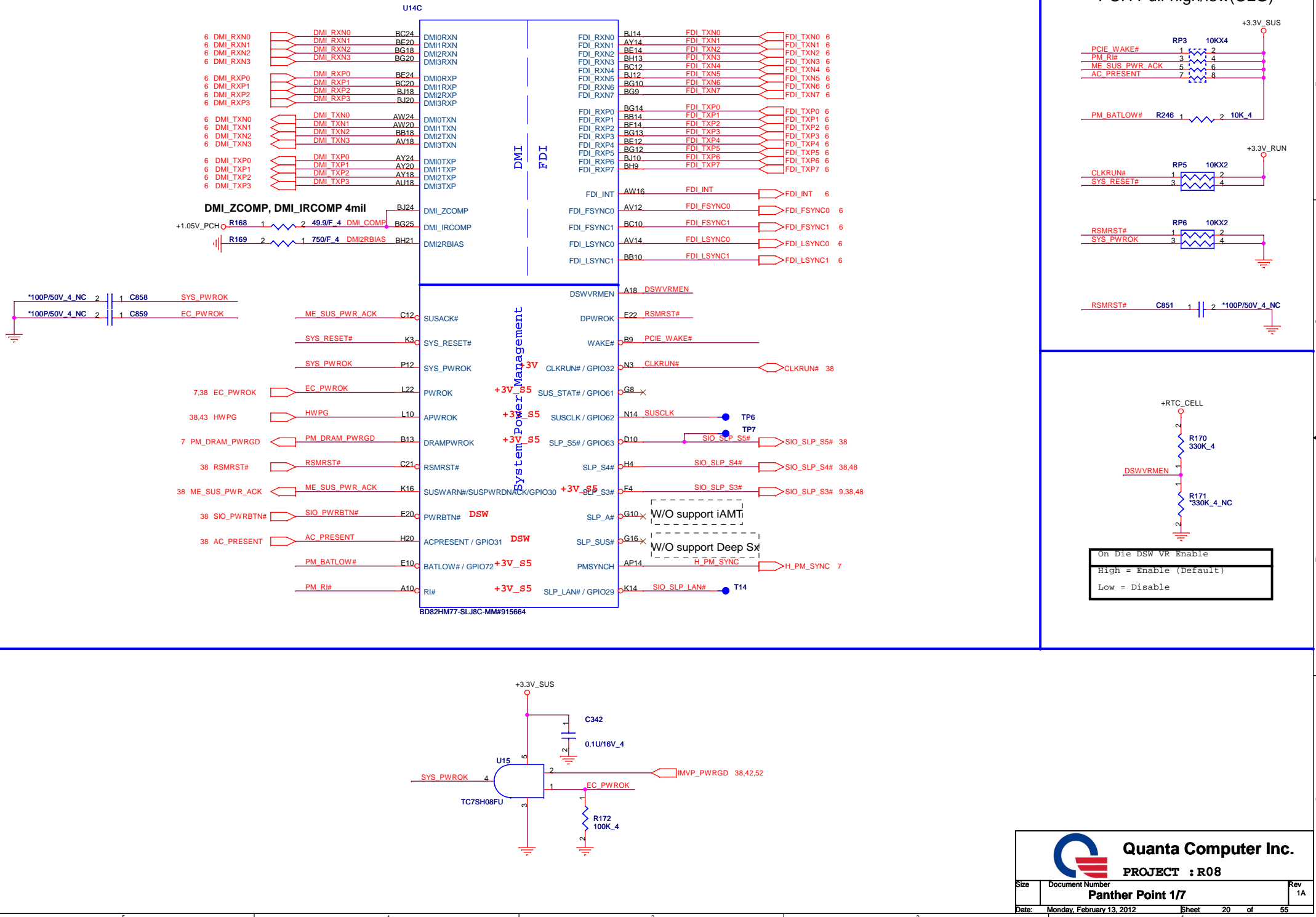
	R148 R149 R162 R163 (MCLK+/MCLK- termination)
N13P-GL	162/F_4 (CS11622FB15)
N13P-GS	80.6/F_4 (CS08062FB19)



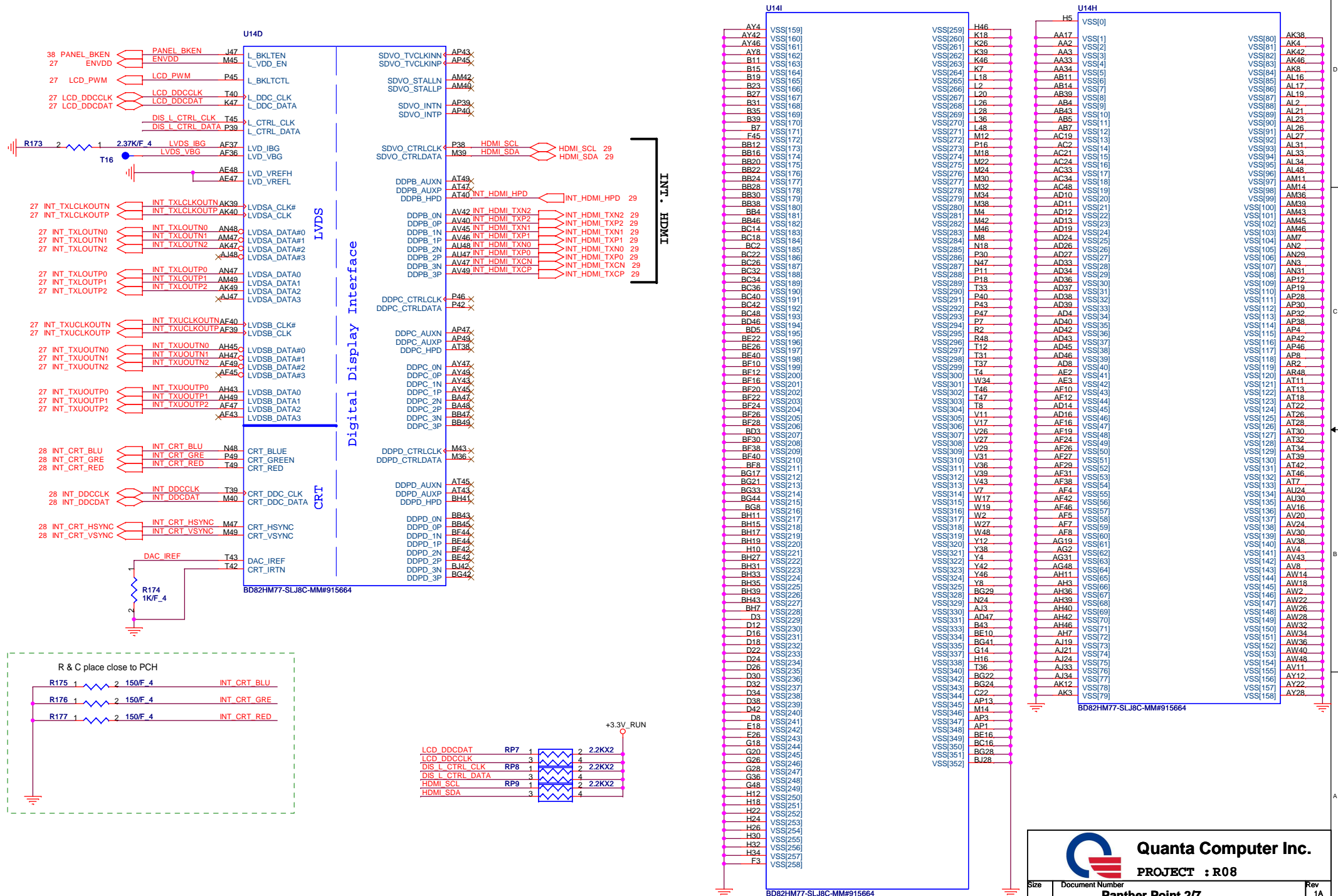
14 VMC_DQ[63..0]
14 VMC_DM[7..0]
14 VMC_WDQS[7..0]
14 VMC_RDQS[7..0]



Cougar Point/Panther Point (DMI,FDI,PM)

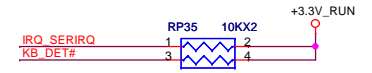
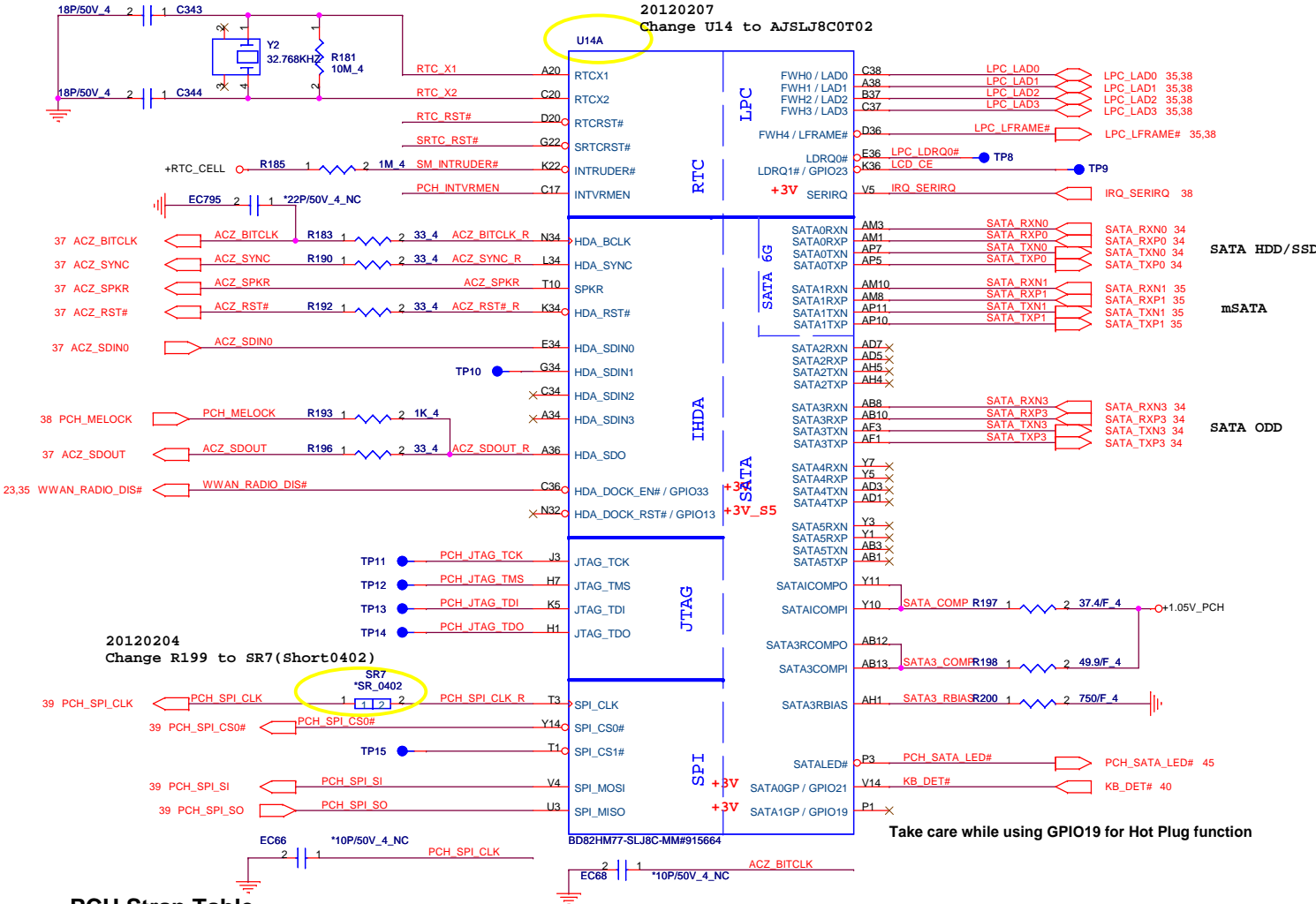


Cougar Point/Panther Point (GND)

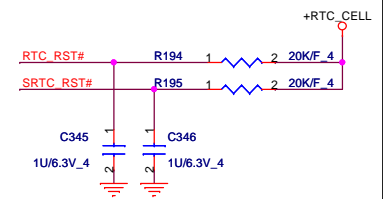


Cougar Point/Panther Point (HDA,JTAG,SATA)

20120204
Change U14 to AJ0QPEG0T07(WINCON)
20120207
Change U14 to AJSLJ8C0T02



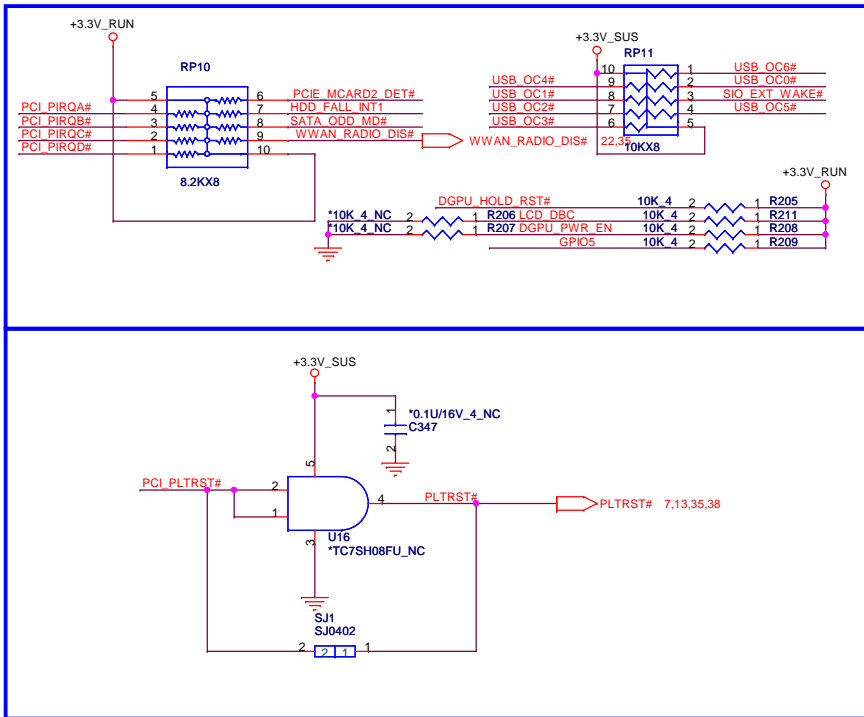
MP remove(Intel)(JTAG)



PCH Strap Table

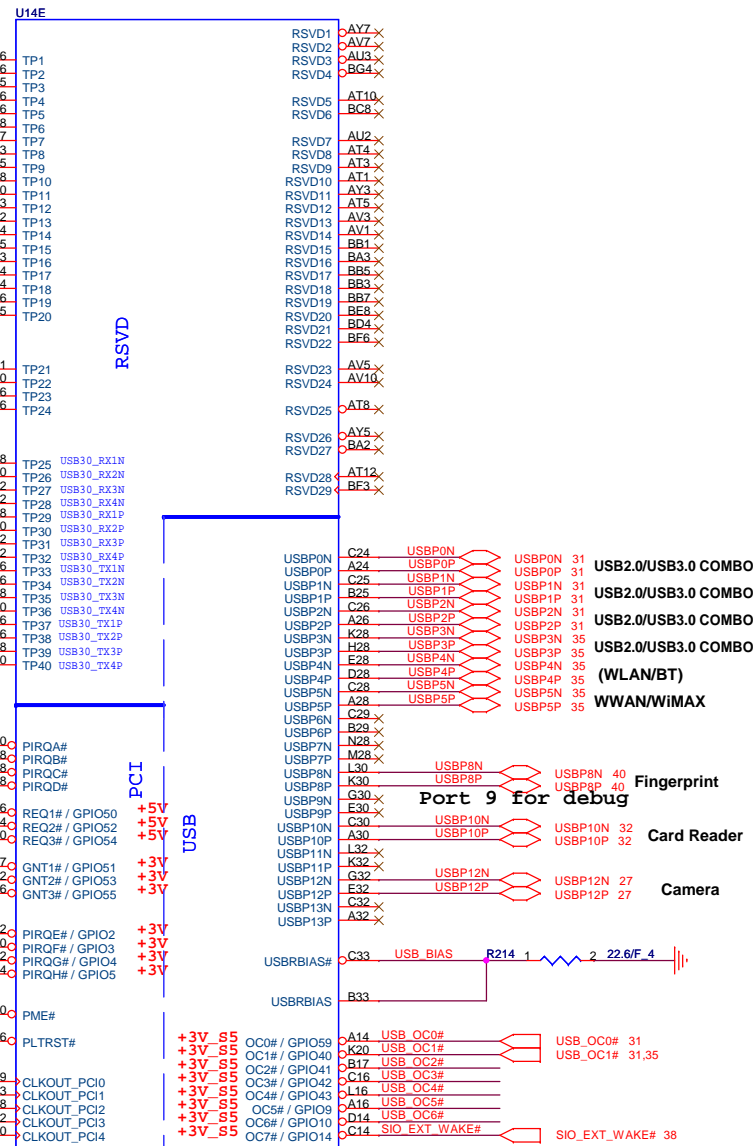
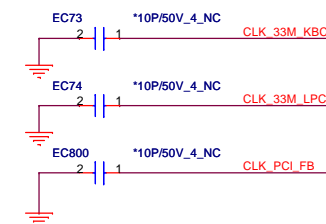
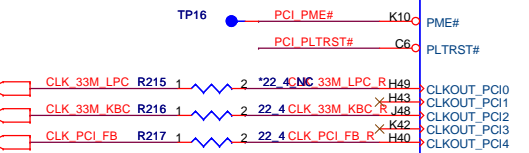
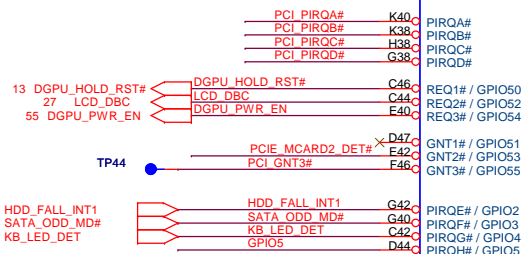
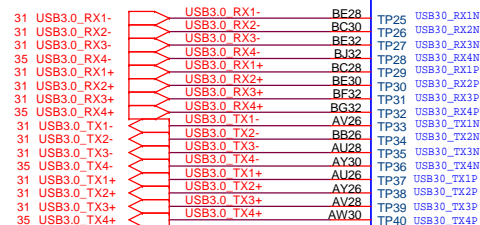
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL ○R203 1 2 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS ○R204 1 2 1K 4 ACZ_SYNC_R

Cougar Point-M/Panther Point (PCI,USB,NVRAM)



Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><td>Bit 0</td><td>Bit 1</td><td>Boot Location</td></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]												
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									

USB3.0

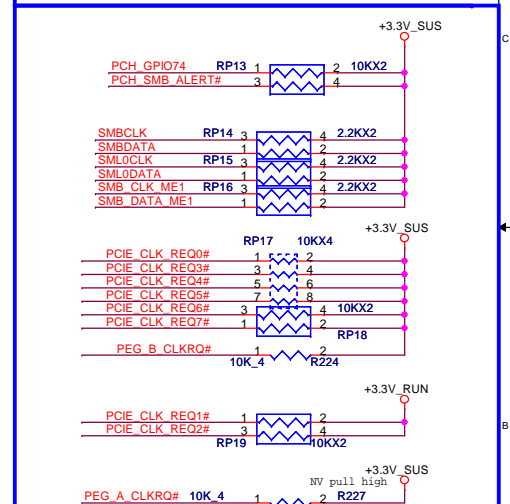
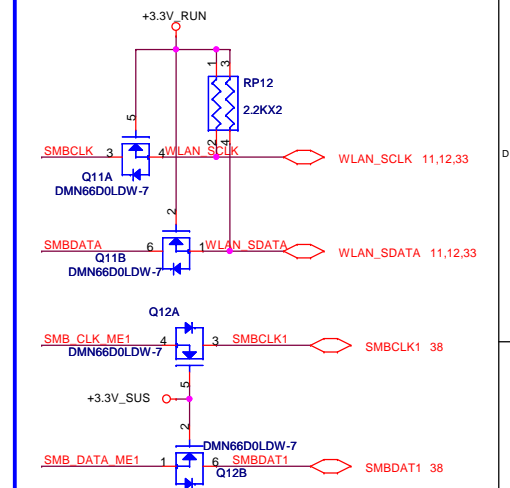


U14B Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



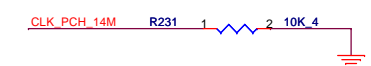
	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 / GPIO64	• 33 / 27 / 48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)

Stuff for Integrated CLK Gen Mode

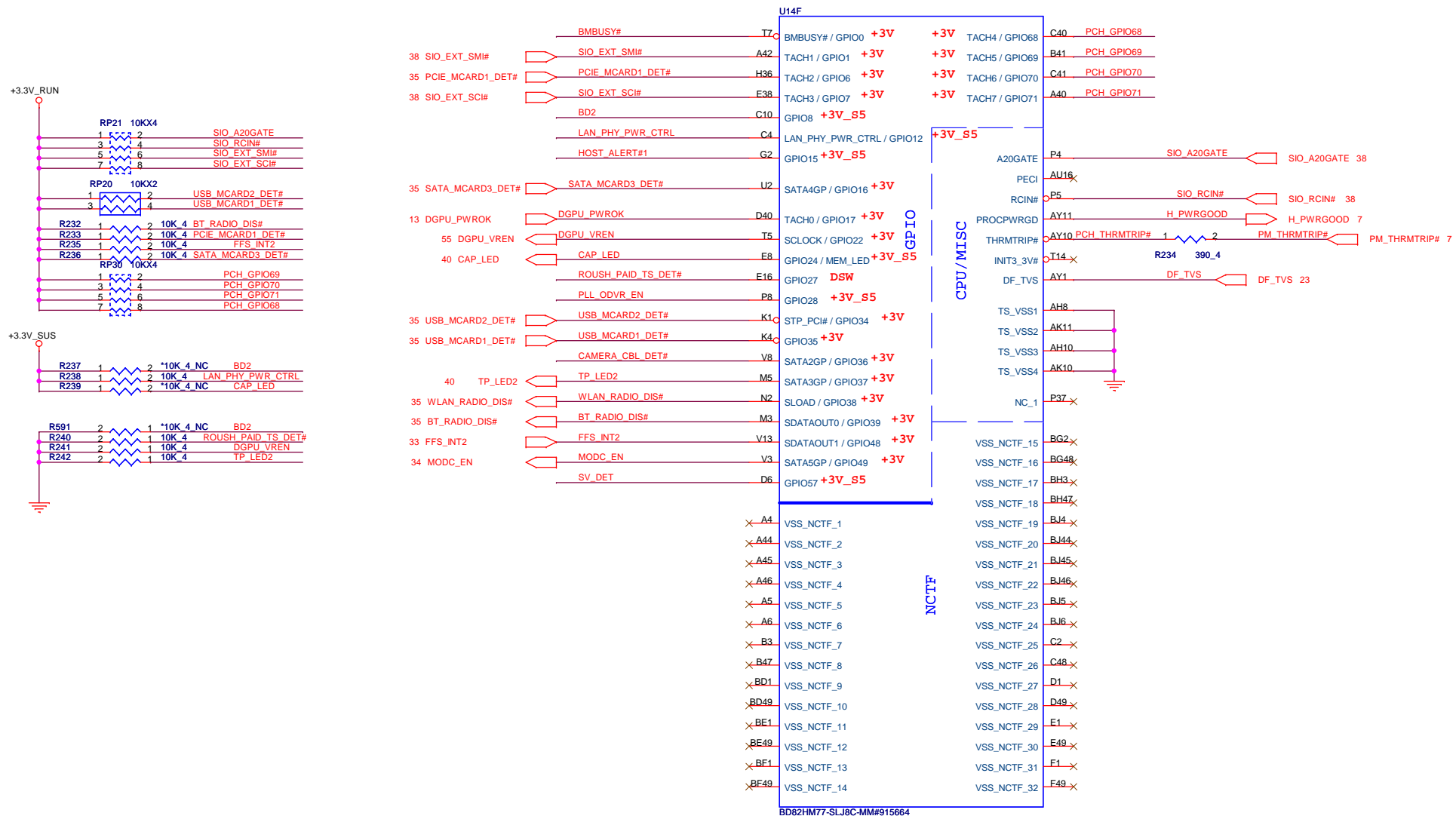
**Quanta Computer Inc.**

PROJECT : R08

Panther Point 5/7

Size	Document Number	Rev
	Panther Point 5/7	1A
Date:	Monday, February 13, 2012	Sheet 24 of 55

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

SGPIO

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

HOST ALERT#1

SV_DET

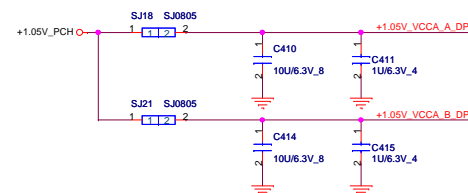
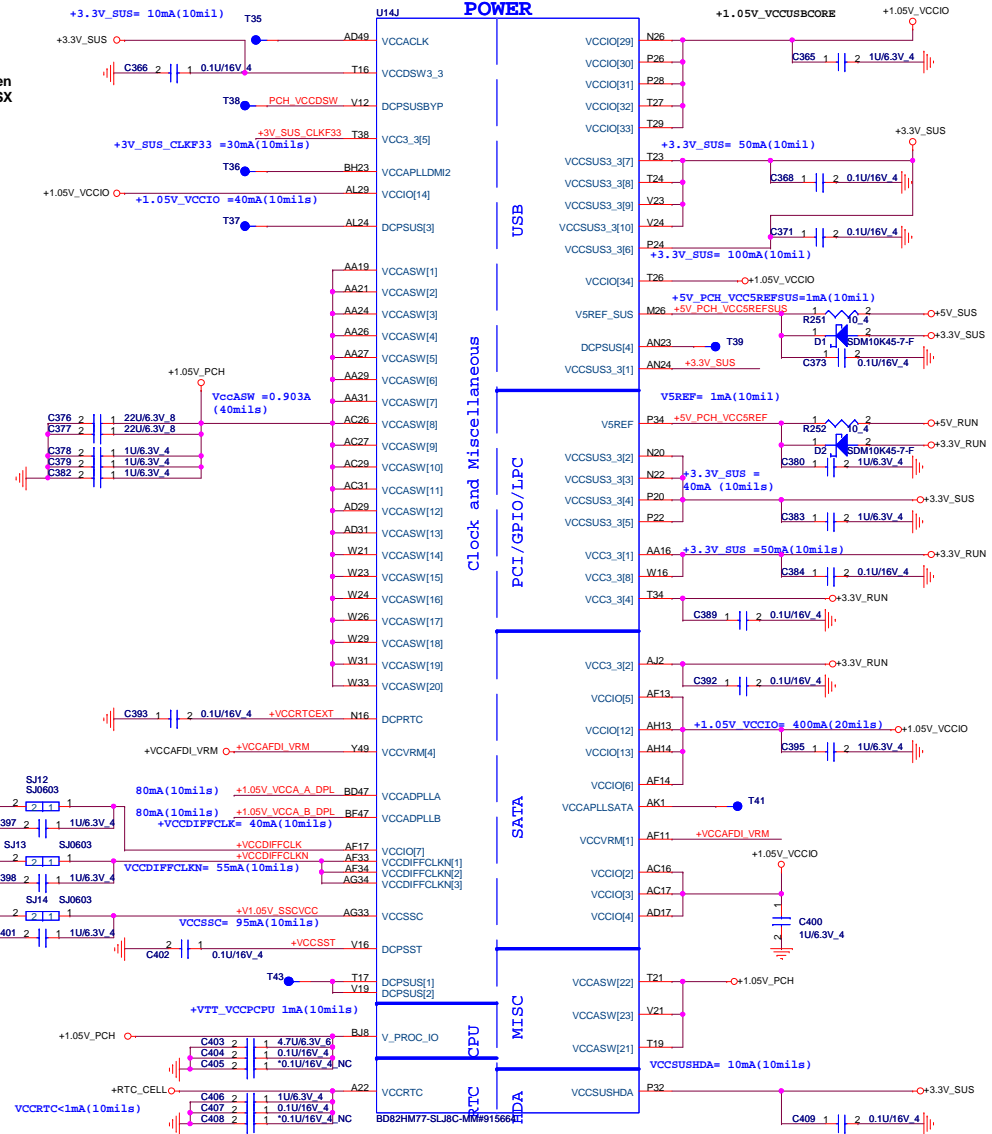
Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

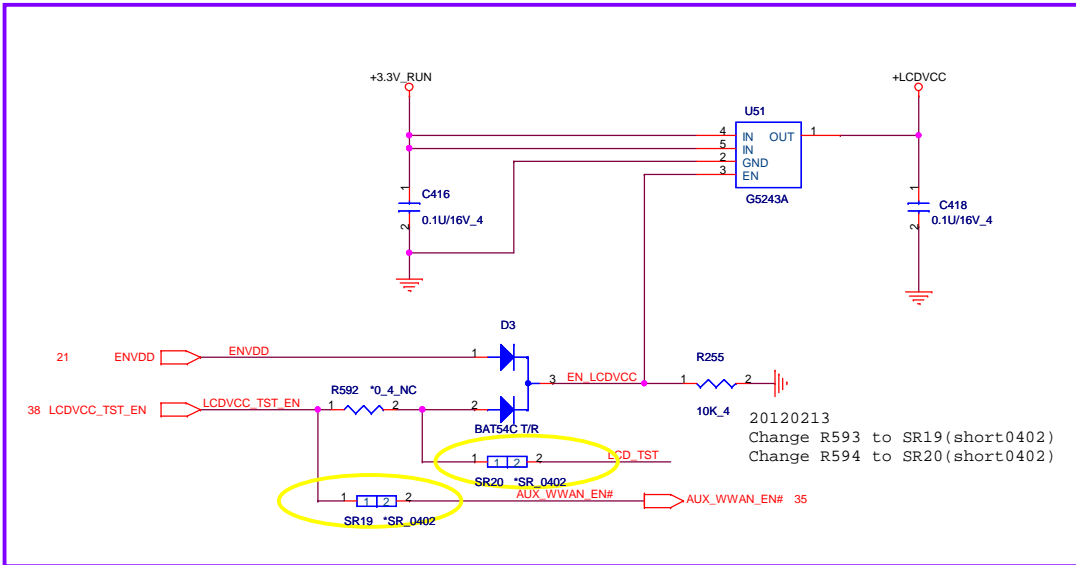
MFG-TEST

Quanta Computer Inc.
PROJECT : R08

Size	Document Number	Rev
	Panther Point 6/7	1A
Date:	Monday, February 13, 2012	Sheet 25 of 55

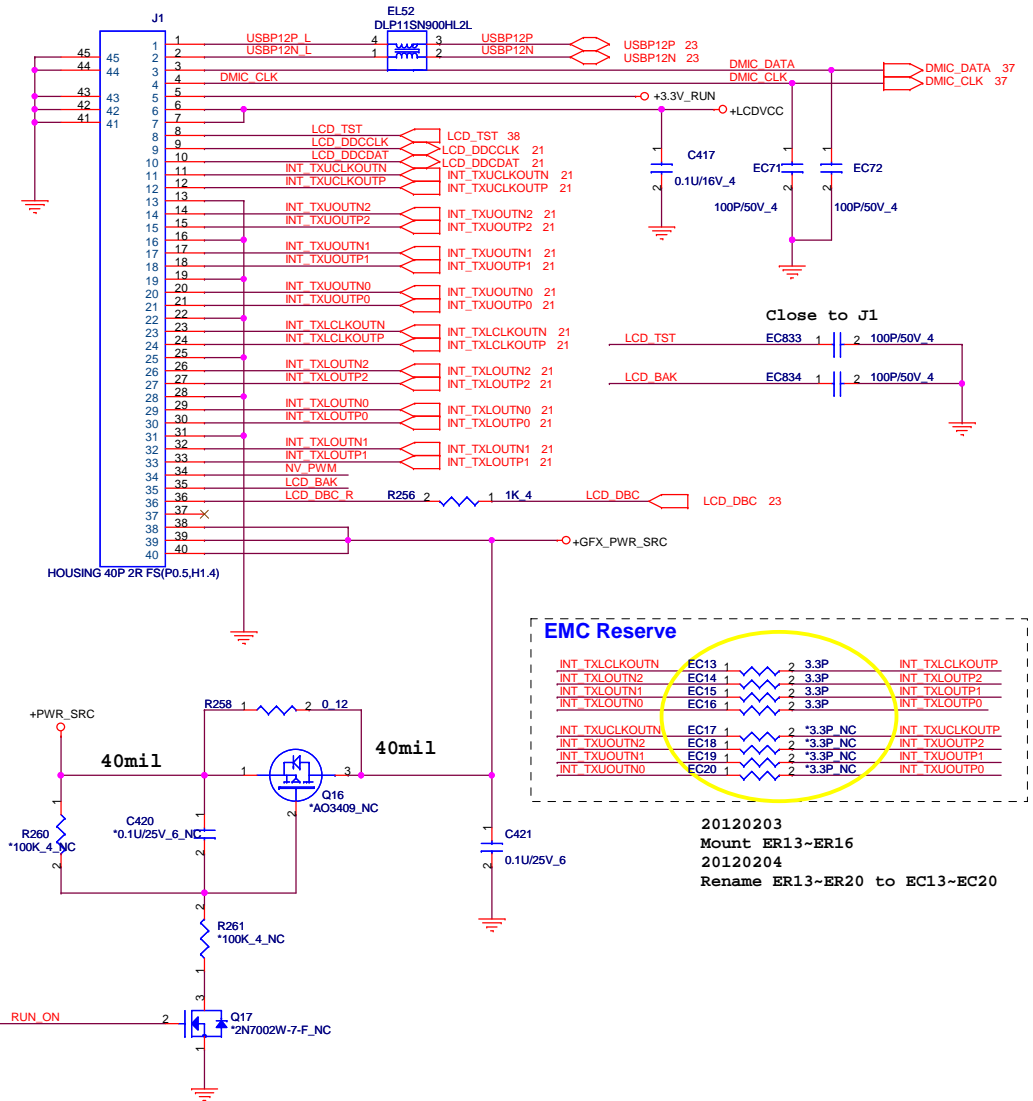
Cougar Point/Panther Point (POWER)



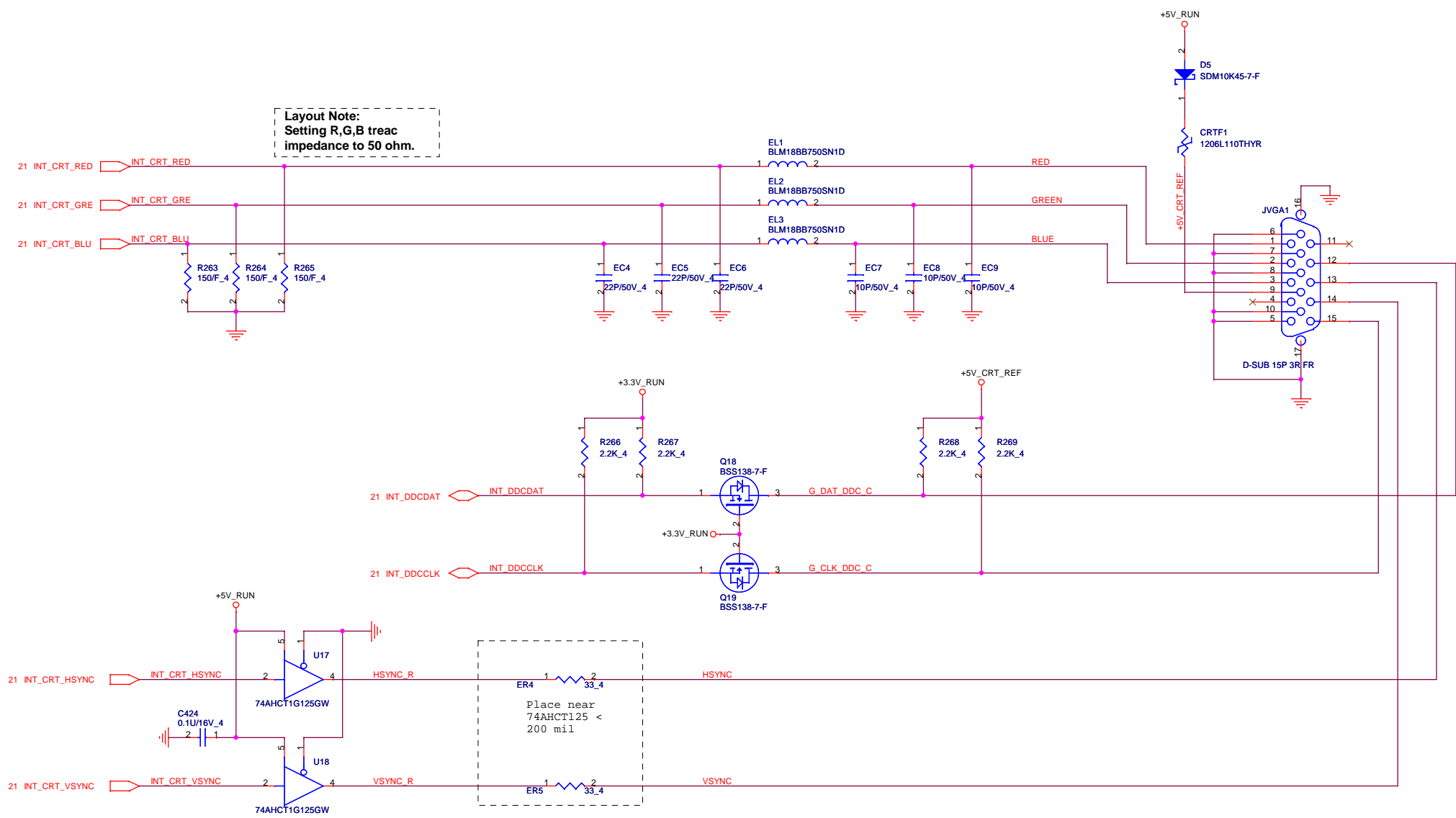


Backlight Enable

Brightness Control



Layout Note:
Setting R,G,B treac
impedance to 50 ohm.

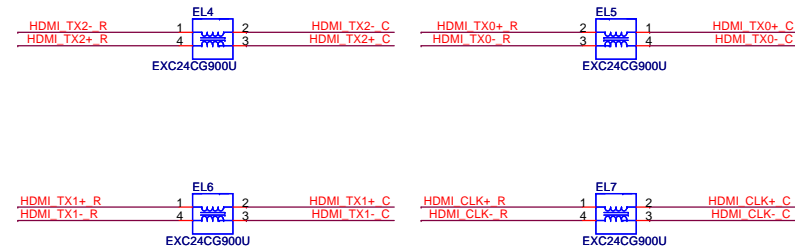


Place near
74AHCT125 <
200 mil

HDMI

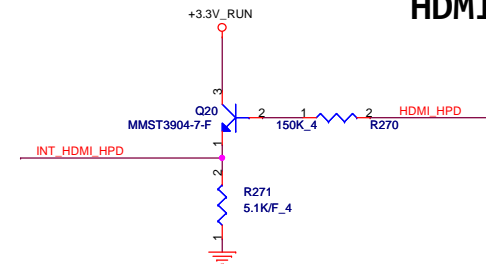
21 INT_HDMI_TXP2	INT_HDMI_TXP2	C425	1	2	0.1U/16V_4	HDMI TX2+ R
21 INT_HDMI_TXN2	INT_HDMI_TXN2	C426	1	2	0.1U/16V_4	HDMI TX2- R
21 INT_HDMI_TXP1	INT_HDMI_TXP1	C427	1	2	0.1U/16V_4	HDMI TX1+ R
21 INT_HDMI_TXN1	INT_HDMI_TXN1	C428	1	2	0.1U/16V_4	HDMI TX1- R
21 INT_HDMI_TXP0	INT_HDMI_TXP0	C429	1	2	0.1U/16V_4	HDMI TX0+ R
21 INT_HDMI_TXN0	INT_HDMI_TXN0	C430	1	2	0.1U/16V_4	HDMI TX0- R
21 INT_HDMI_TXCP	INT_HDMI_TXCP	C431	1	2	0.1U/16V_4	HDMI CLK+ R
21 INT_HDMI_TXCN	INT_HDMI_TXCN	C432	1	2	0.1U/16V_4	HDMI CLK- R
21 HDMI_SCL	HDMI_SCL					
21 HDMI_SDA	HDMI_SDA					
21 INT_HDMI_HPD	INT_HDMI_HPD					

Reserve for EMI and close to HDMI CONN



HDMI_HPD spec VinH_min=2.0V

HDMI HPD

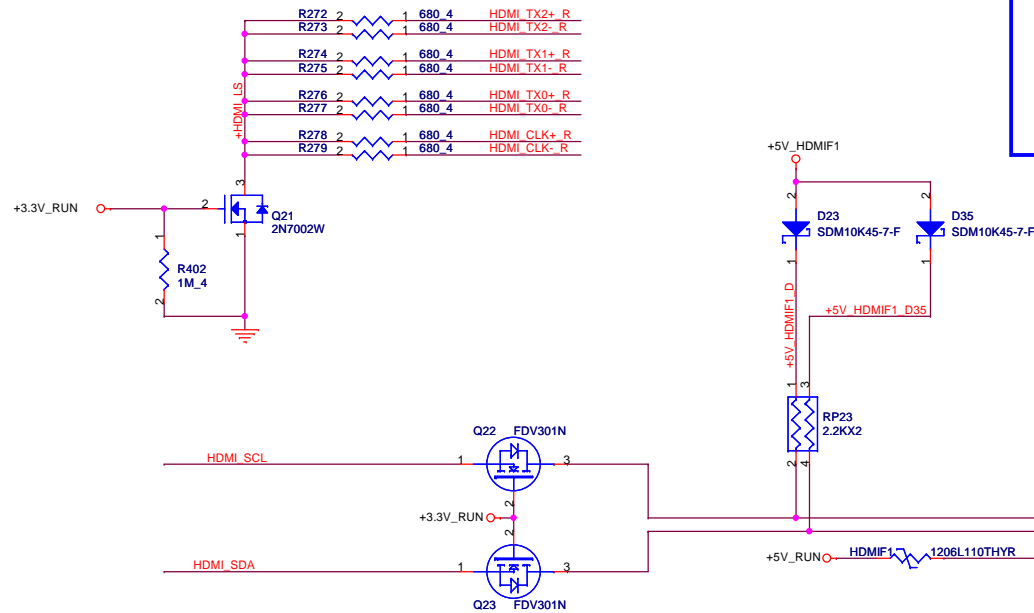


$$IB = (5V - 0.7V) / (150K + (70 + 1) 5.1K) = 8.4\mu A$$

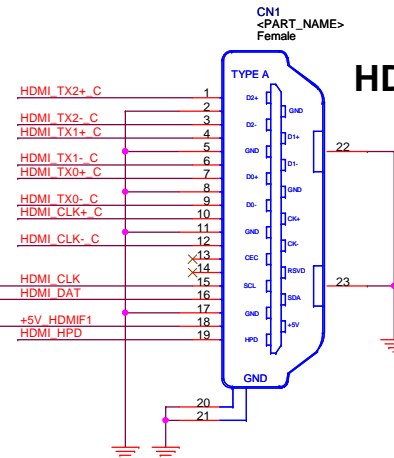
$$IE = (1 + 70) \times 8.4\mu A = 596.4\mu A$$

$$VE = 596.4\mu A \times 5.1K = 3.04V$$

$$B = 70$$



HDMI Conn.



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PROJECT : R08

	A	B	C	D	E
4					
3					
2					
1					



Quanta Computer Inc.

PROJECT : R08

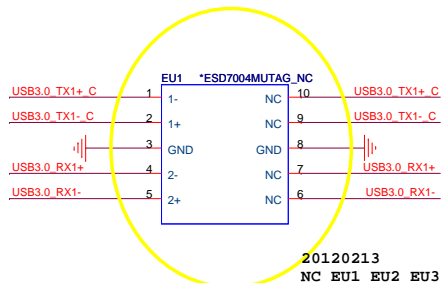
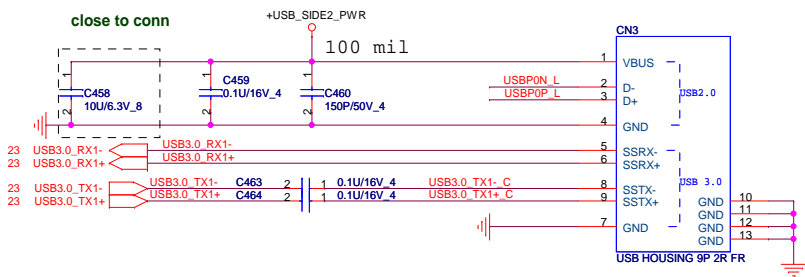
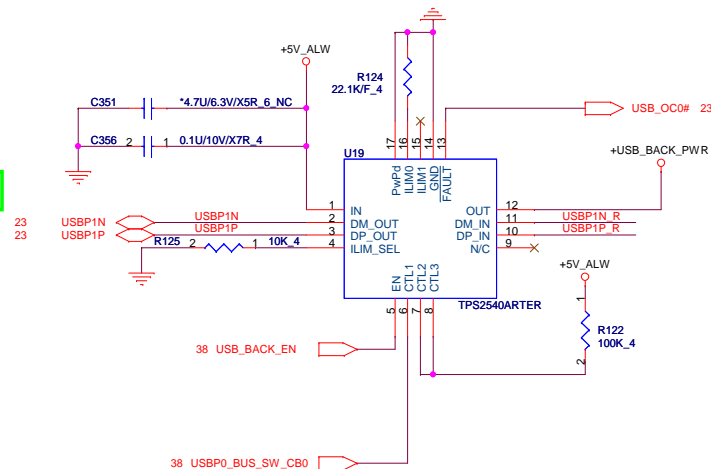
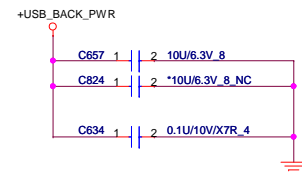
Size	Document Number	Rev
	NA	1A
Date:	Monday, February 13, 2012	Sheet 30 of 55

USB Power share

USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A

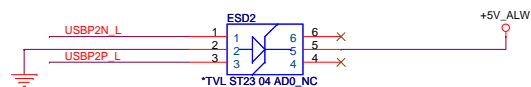
	R109	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

Applied Now

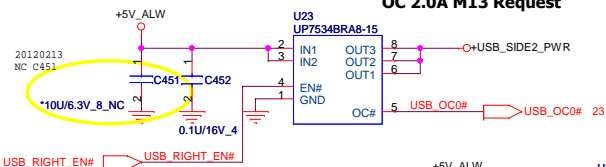


ESD Function

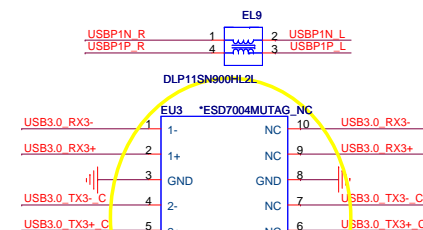
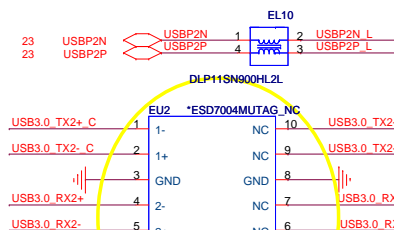
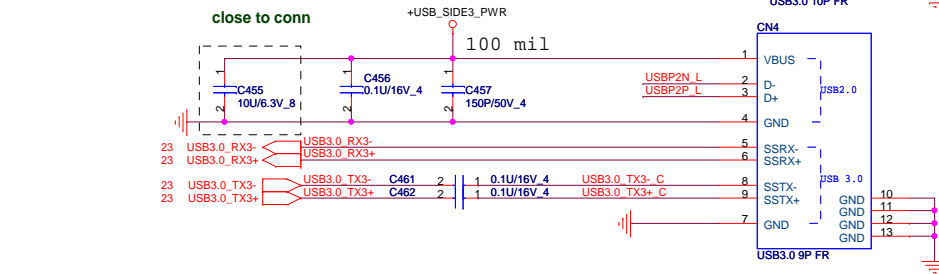
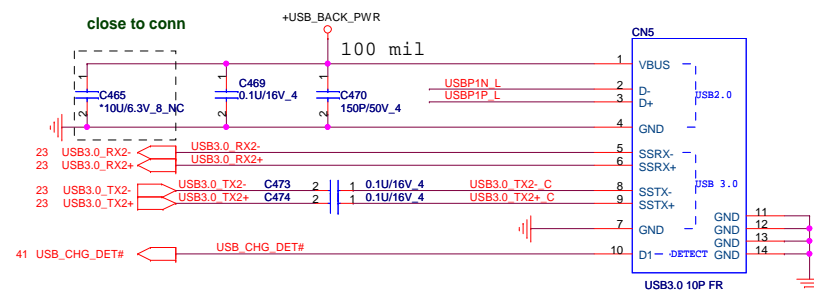
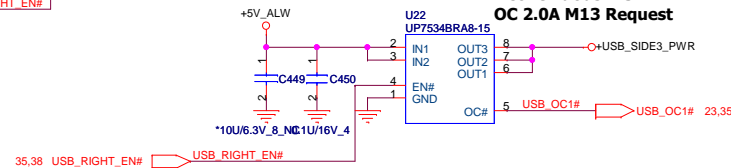
Place ESD diodes as close as USB connector.



I continuous 1.5A OC 2.0A M13 Request



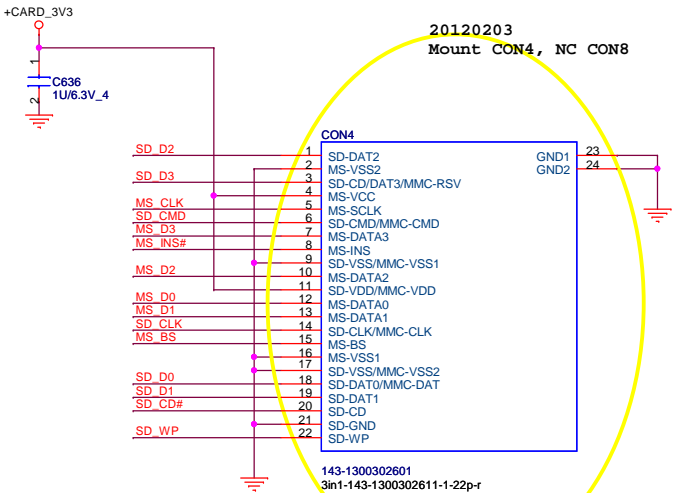
I continuous 1.5A OC 2.0A M13 Request



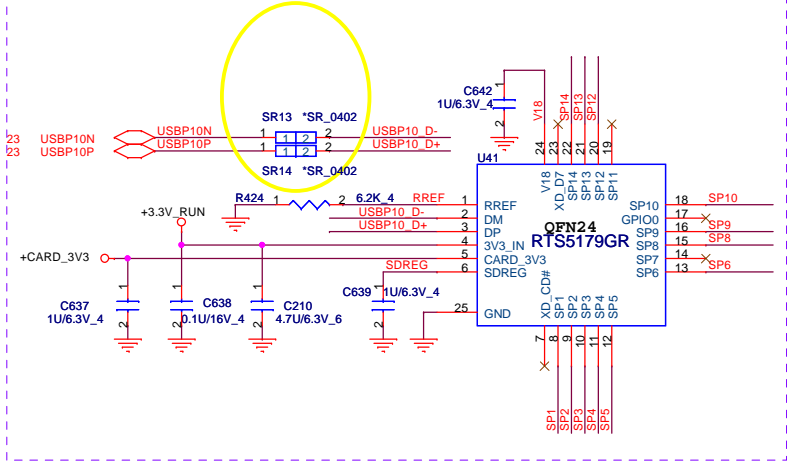
ESD Function

Cardreader (RTS5179GR) Support SD3.0 USH50

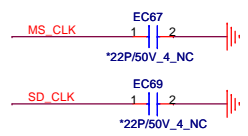
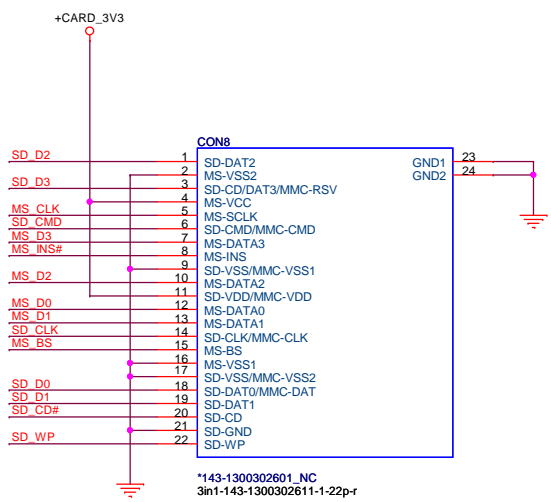
For Vostro Placement(V08,V08A)-Far ODD



20120206
Remove EL47
Change R210 to SR13(short0402)
Change R212 to SR14(short0402)



For INSPIRON Placement (R08,R08A,R08T)-Near ODD

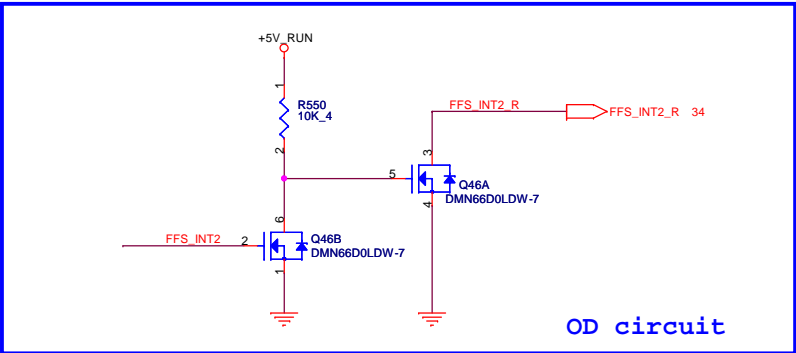


SP1	SD WP	MS CLK
SP2	SD D1	MS INS#
SP3	SD D0	MS D7
SP4	SD D7	MS D3
SP5	SD CD#	
SP6		
SP8	SD CLK	MS D2
SP9	SD D5	MS D0
SP10	SD CMD	
SP12	SD D3	MS D1
SP13	SD D2	MS D5
SP14		MS BS

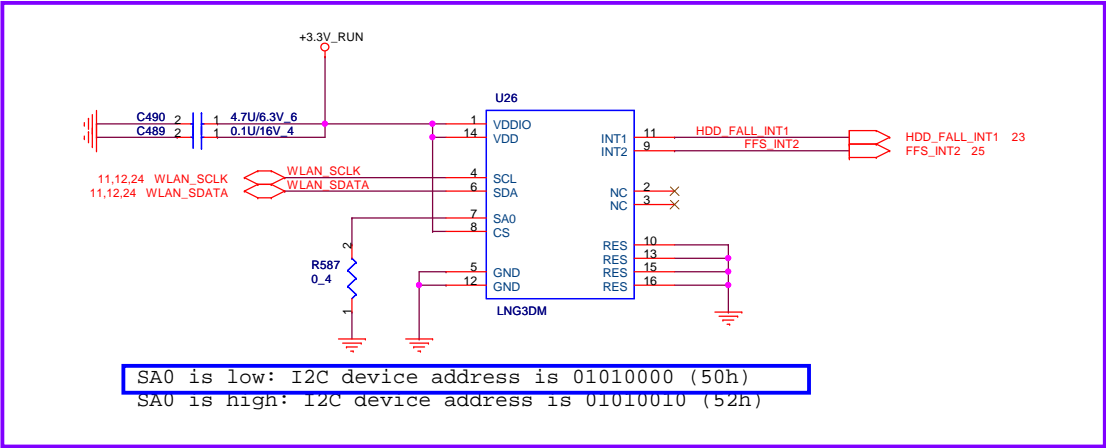
Share Pin

3-axis Fall Sensor

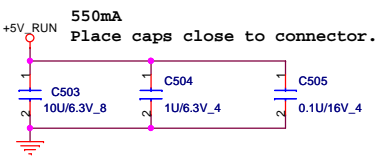
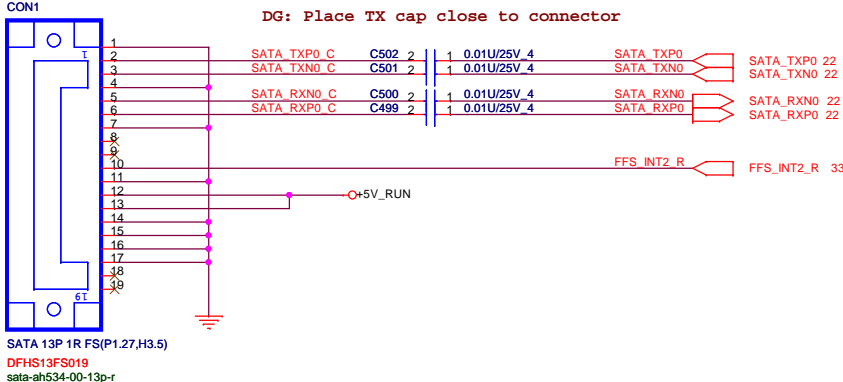
If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit



20120203
Mount Function code "FFS" part

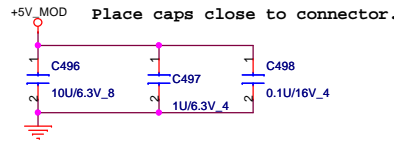
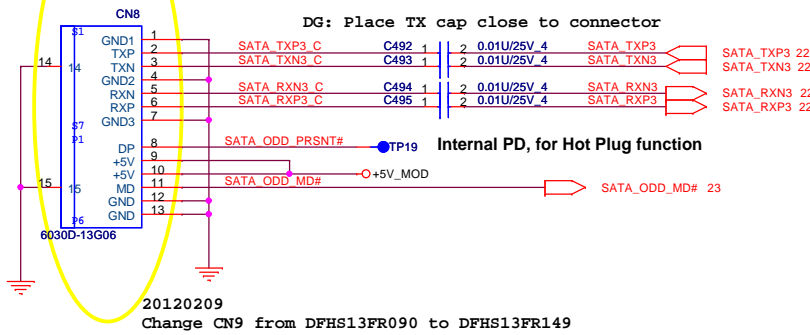


HDD

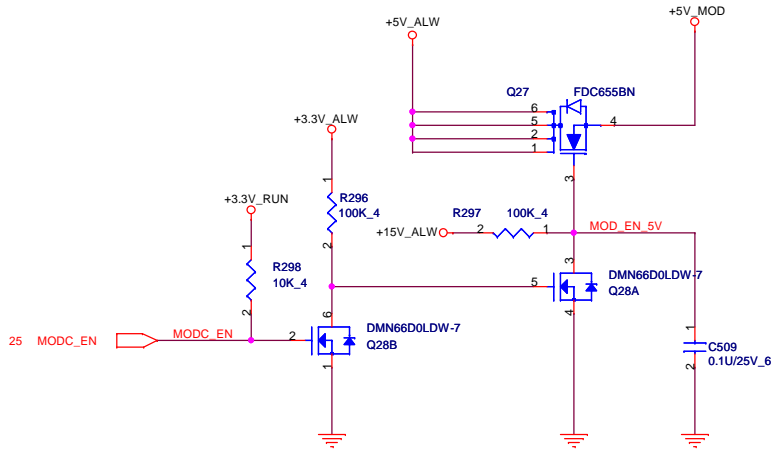


ODD

ODD Connector



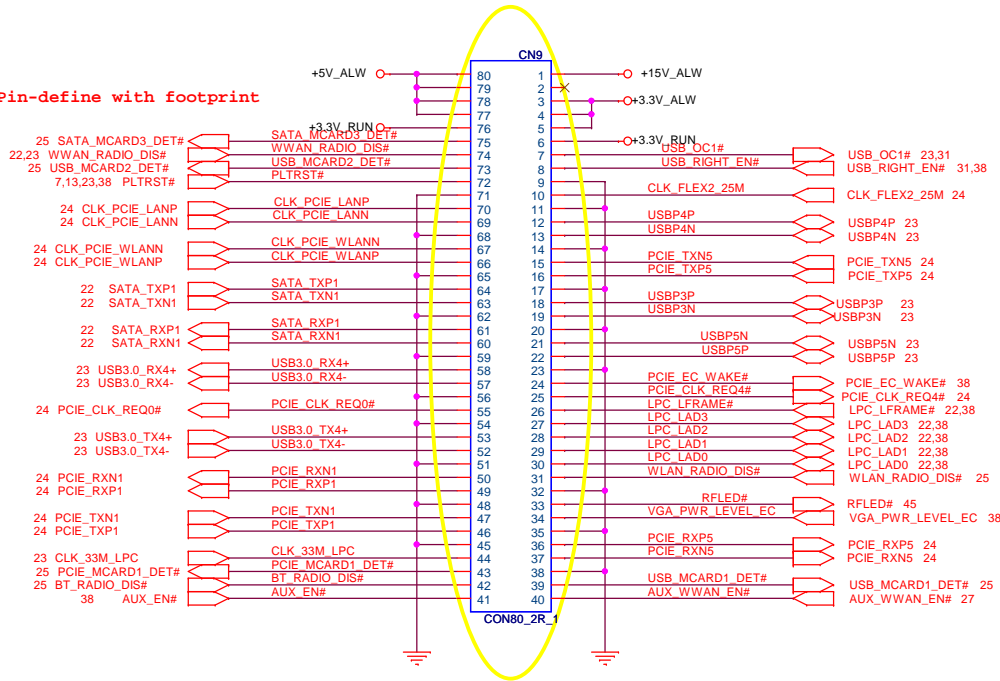
Support Zero power ODD



20120203

Change CN9 footprint from "88069-8001b-bs-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"

Check Pin-define with footprint

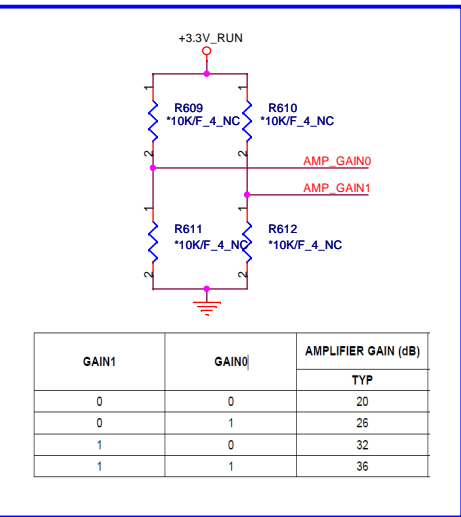
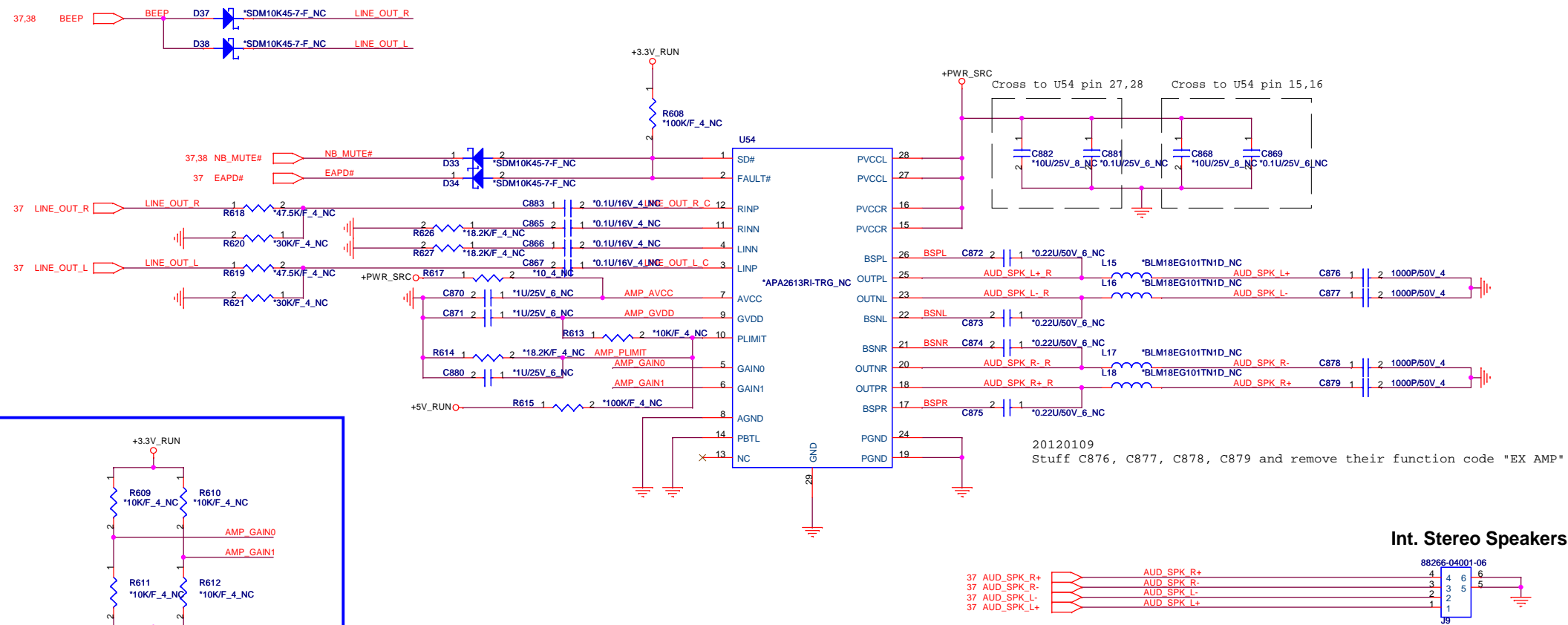


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PROJECT : R08

Size	Document Number	Rev
	BTB CONN	3A
Date:	Monday, February 13, 2012	Sheet 35 of 55

ANPEC APA2613 is P2P to TI TPA3113 Default use APA2613

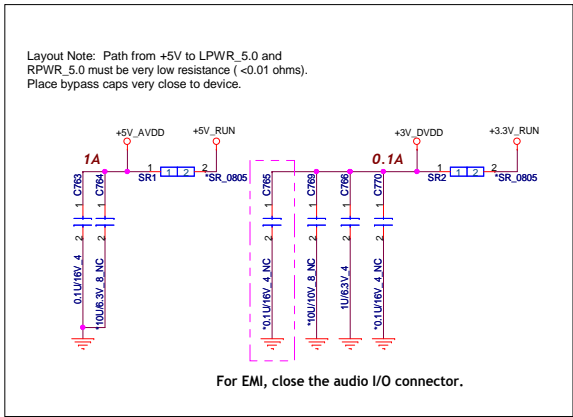
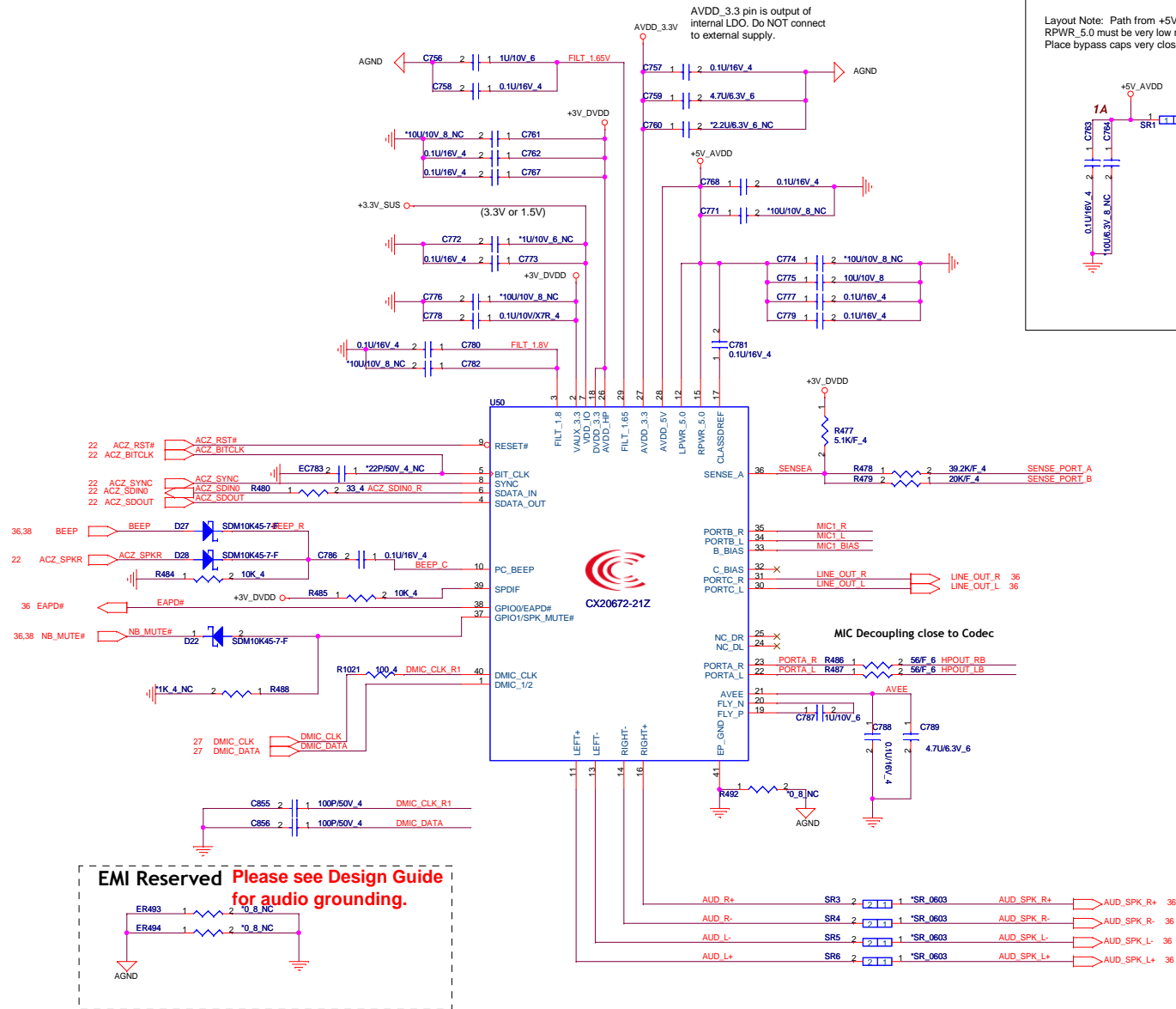


GAIN1	GAIN0	AMPLIFIER GAIN (dB)
		TYP
0	0	20
0	1	26
1	0	32
1	1	36

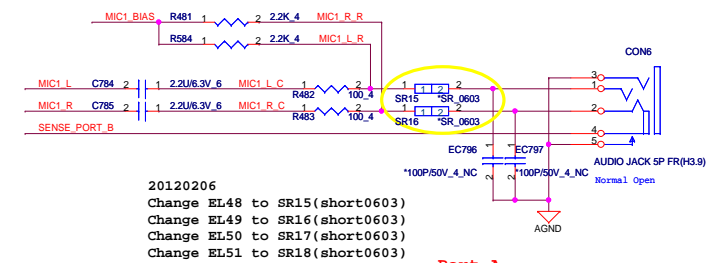
	Amplifier	Function code
R08/R08A/V08/V08A	CODEC CX20672	Mount "IN AMP"
R08T	APA2613 or TPA3113	Mount "EX AMP"

Int. Stereo Speakers

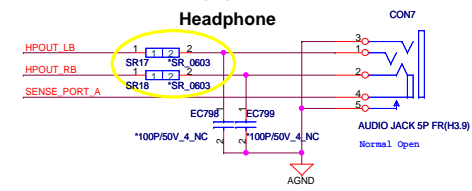


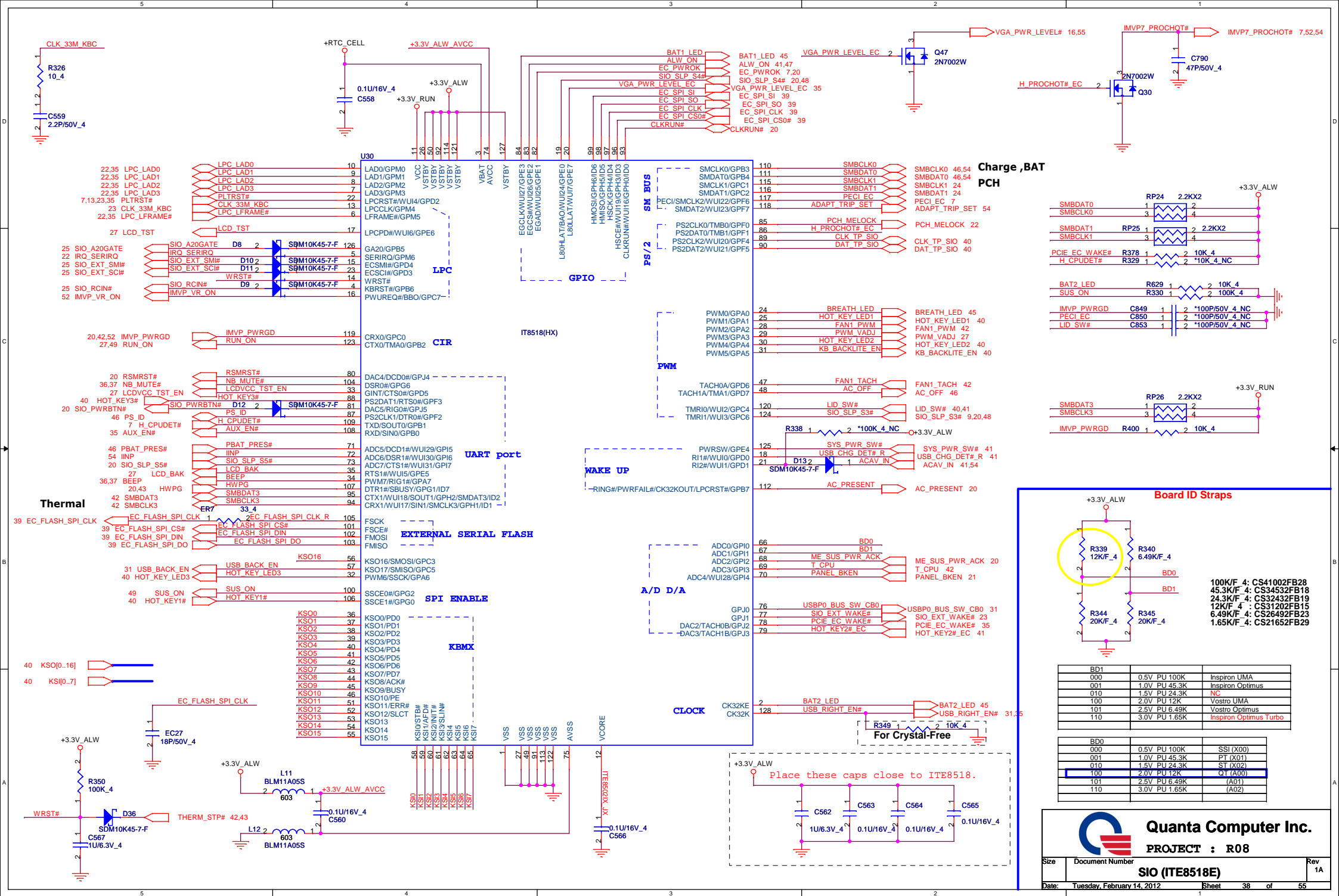


Port B
External Stereo microphone



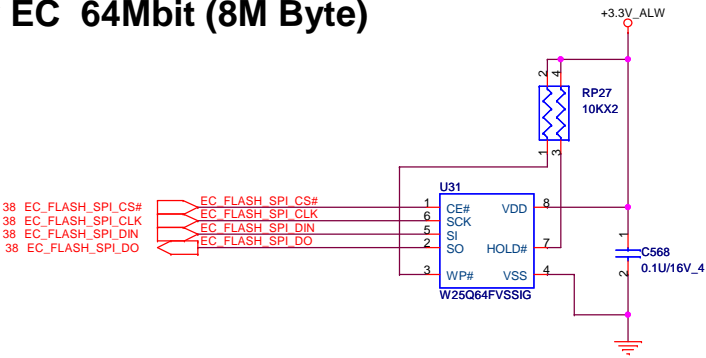
Port A
Headphone



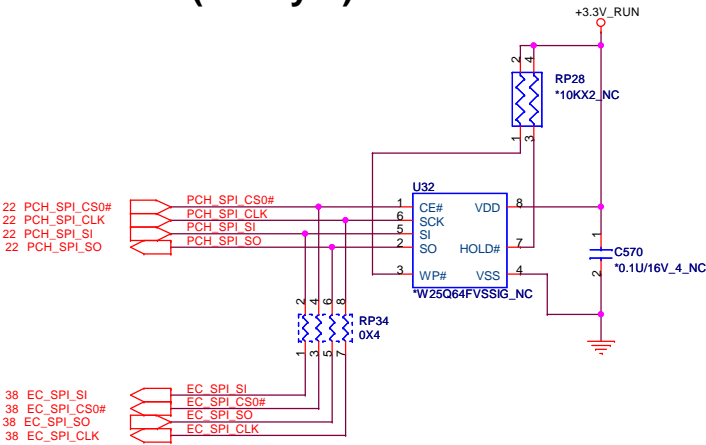


FLASH / RTC

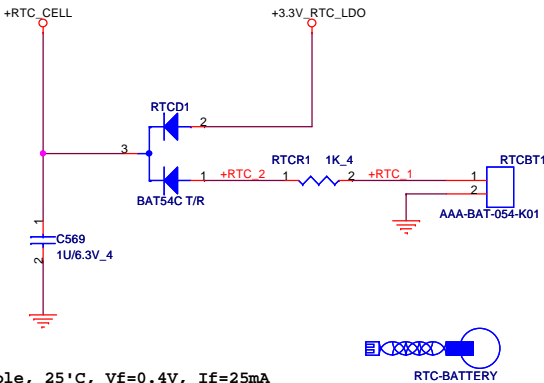
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)



RTC



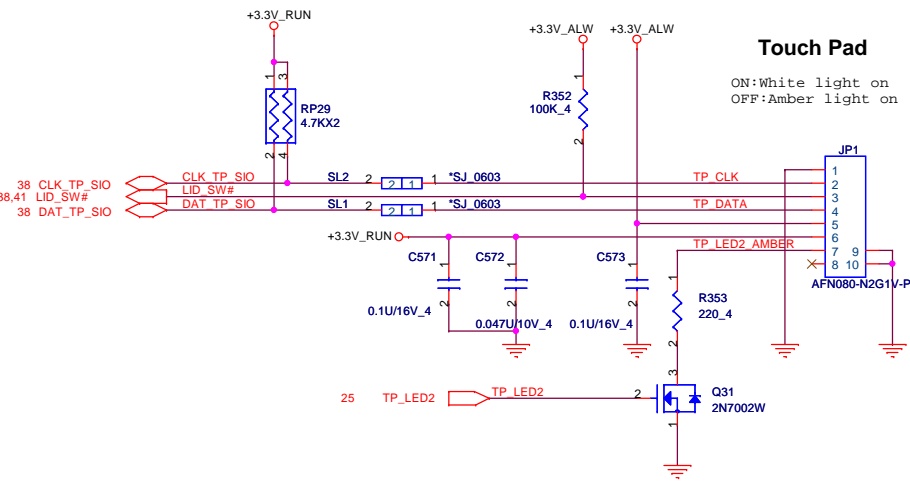
Double, 25°C, Vf=0.4V, If=25mA
one, 25°C, Vf=0.35V, If=15.8mA



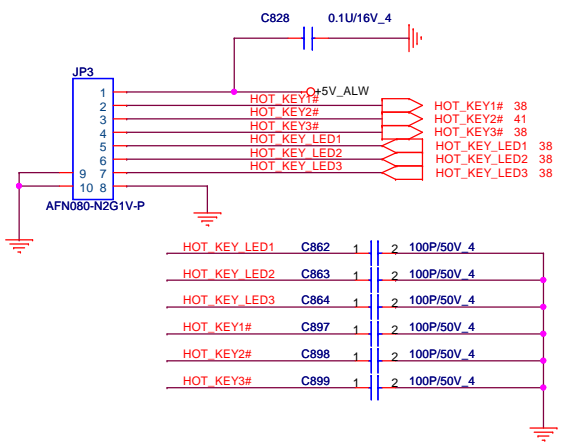
Quanta Computer Inc.

PROJECT : R08

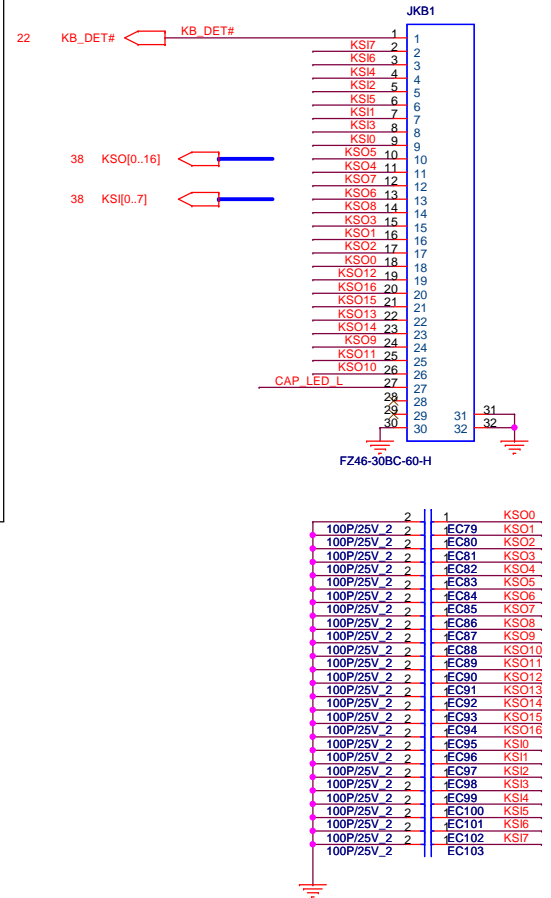
TP CONNECTOR



HotKey CONN

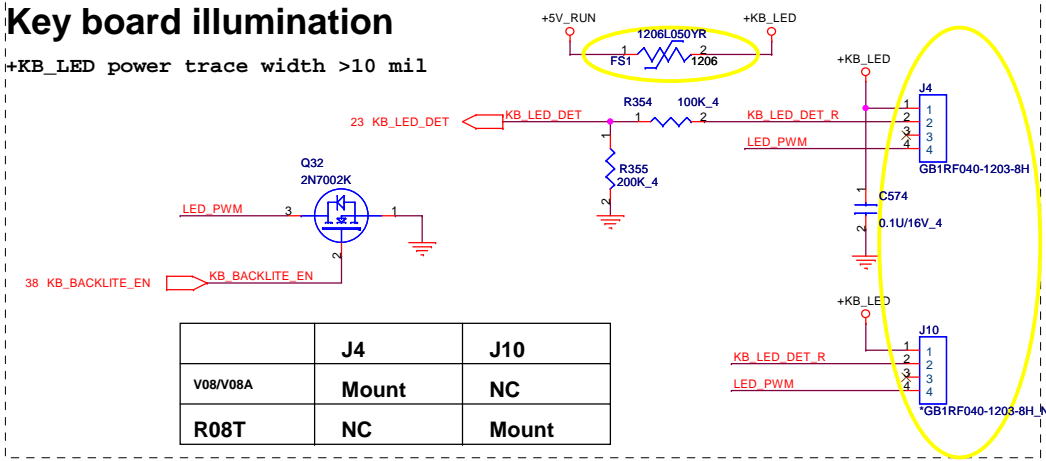


KB CONN



Key board illumination

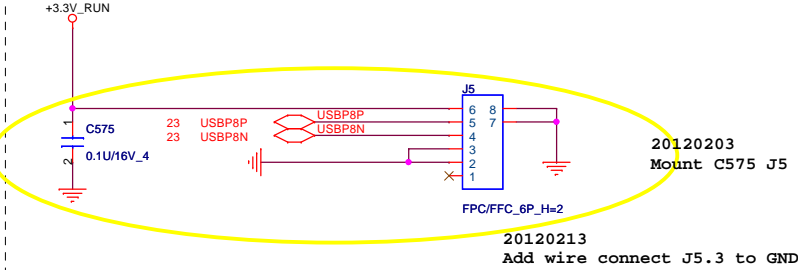
+KB_LED power trace width >10 mil



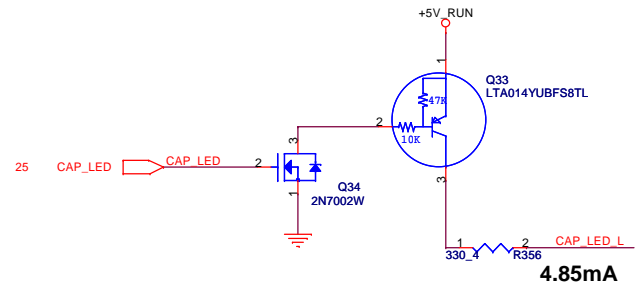
20120206
Change FS1 to SR12(short1206)
20120213
Change SR12 back to FS1

20120203
Mount J4, NC J10

Fingerprint

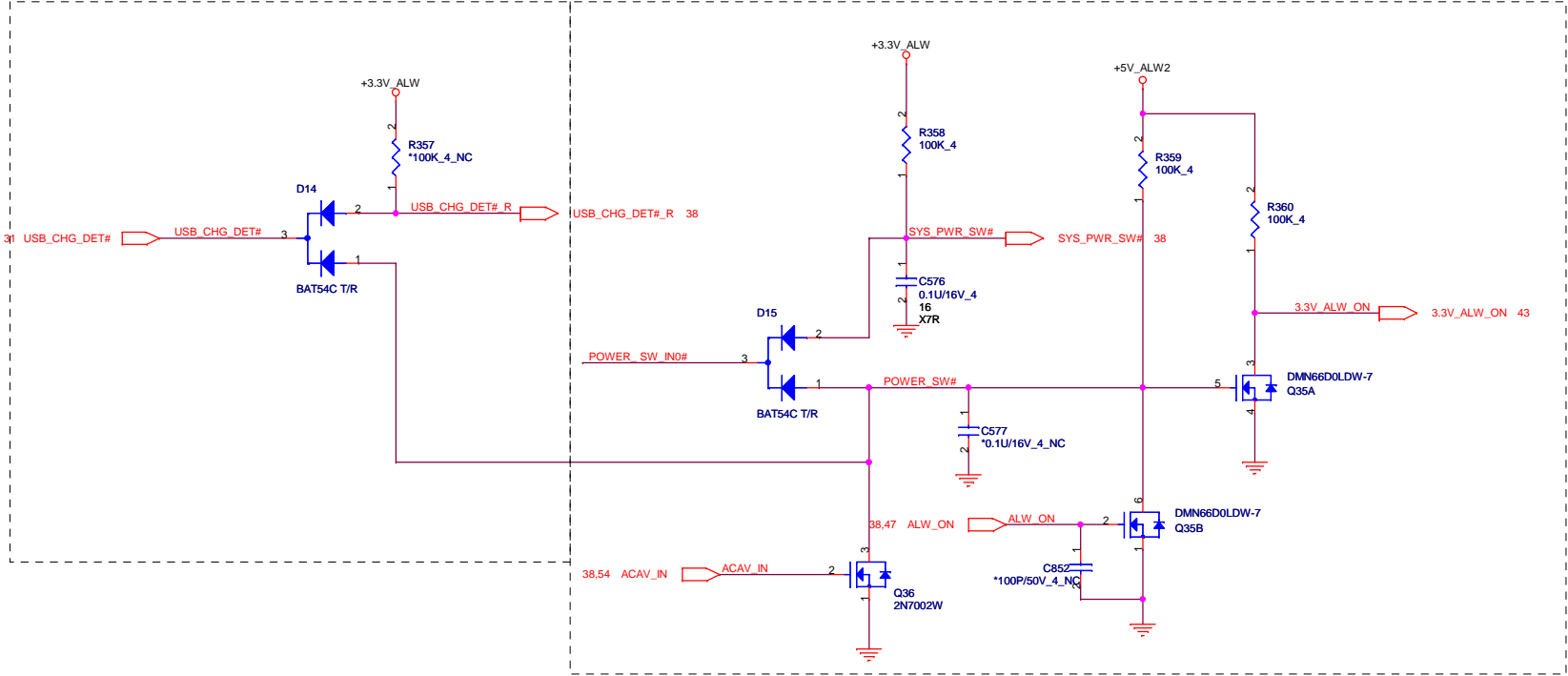


Vi(on_max)= -1.4V
Vi(off_min)=-0.3

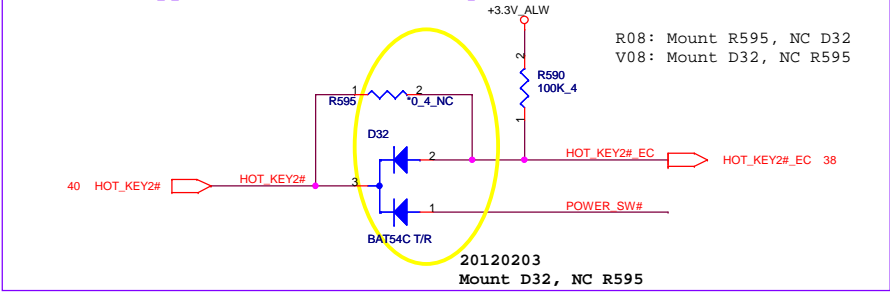


For USB charger usage

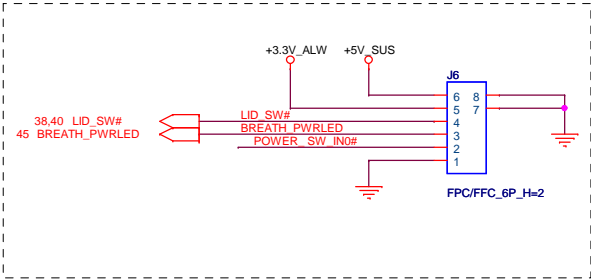
3V ALW ON POWER LOGIC

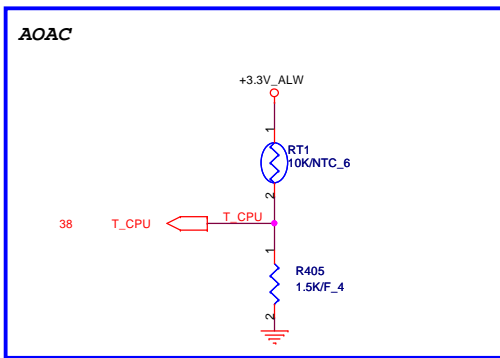


HOT_KEY2 support Pre-Boot Recovery



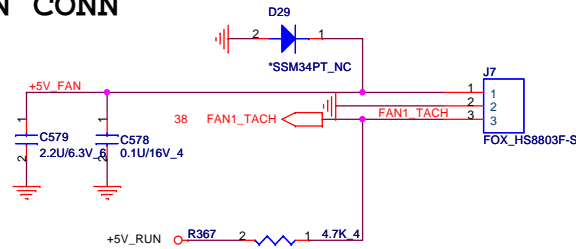
TO PWR button board





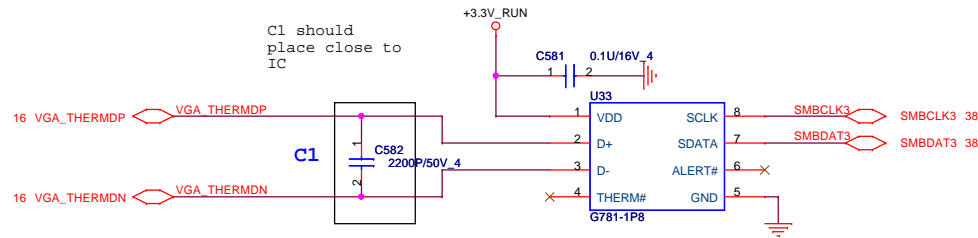
20120203
Mount RT1 R405 for V08A SKU

FAN CONN



G781-1P8

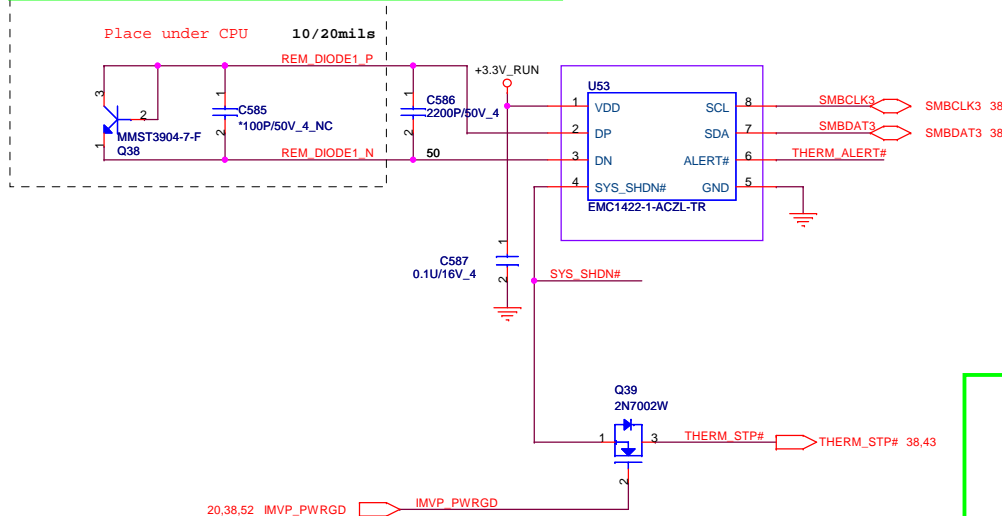
SMBus address is 1001101xb (9Ah) (x is R/W bit).



C1 should place close to IC

THERMAL IC

1. Place C586 close to EMC1422-U1
 2. Place C585 to be close to Q38
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C586, then C585 should be dummy

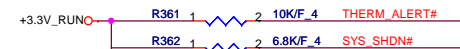


EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	4.7K	77'C	83'C	89'C	95'C	101'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C

CHECK OTP WITH Thermal.

OTP 85 degree C



EMC1422

OTP 85 degree : R361 = 10K, R362 = 6.8K
OTP 90 degree : R361 = 6.8K, R362 = 10K

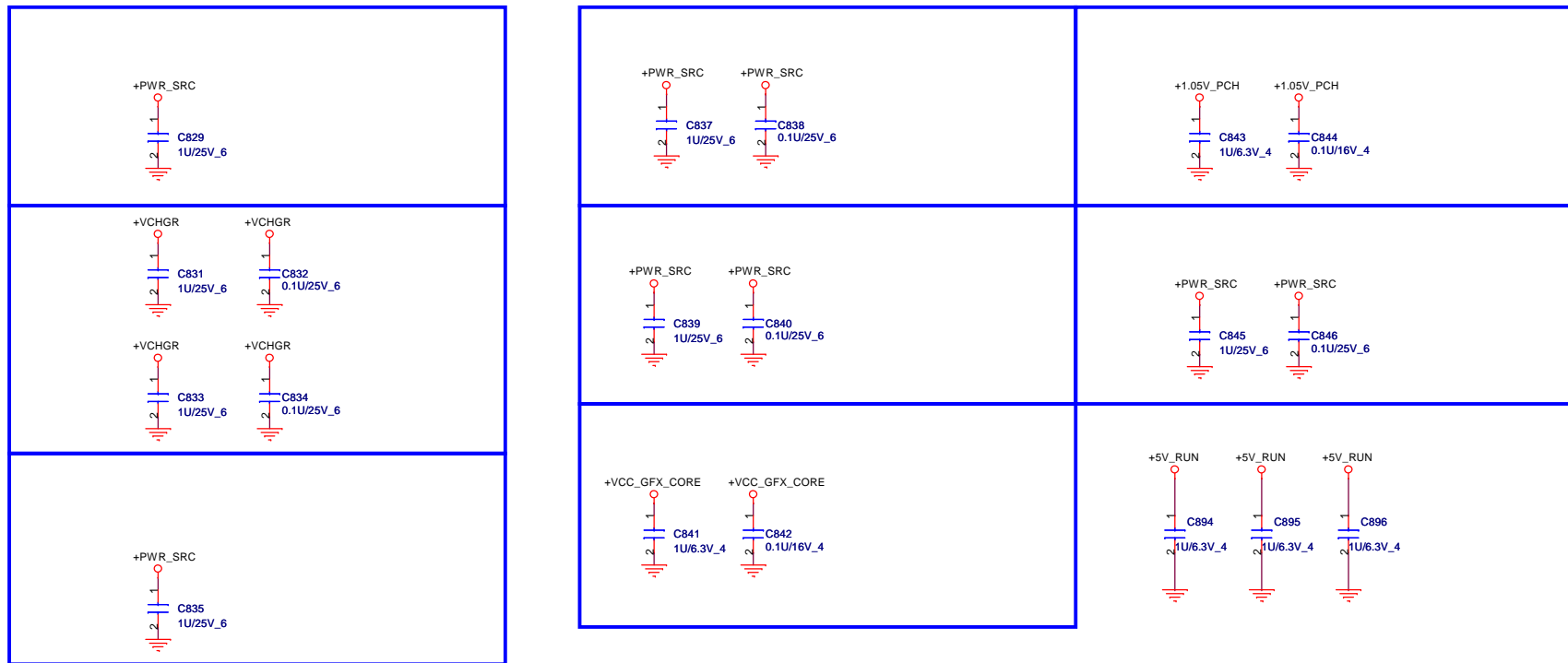
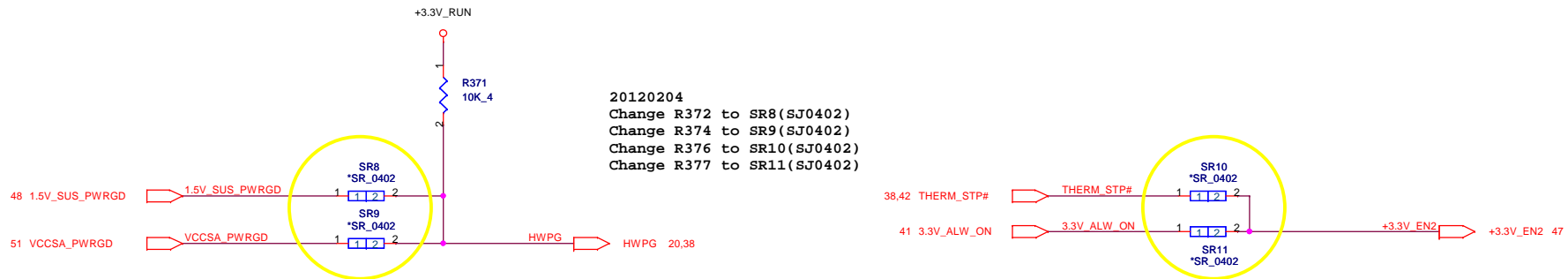
NTC7718W

OTP 85 degree : R361 = 18.7K, R362 = 2K
OTP 91 degree : R361 = 10.5K, R362 = 7.5K

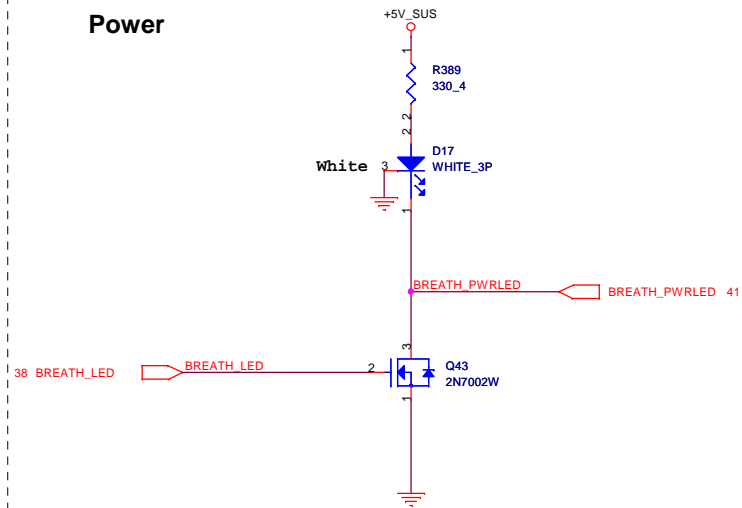


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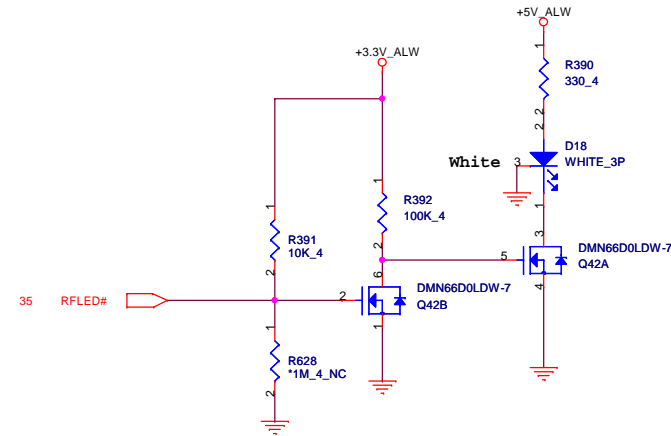
PROJECT : R08



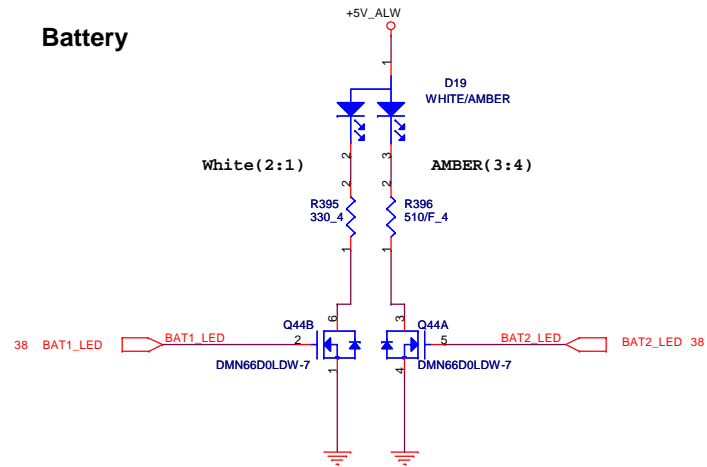
Power



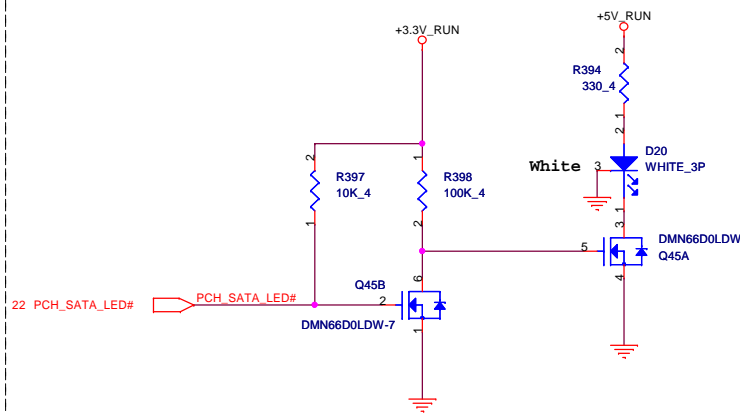
Bluetooth / WLAN on/off LED



Battery



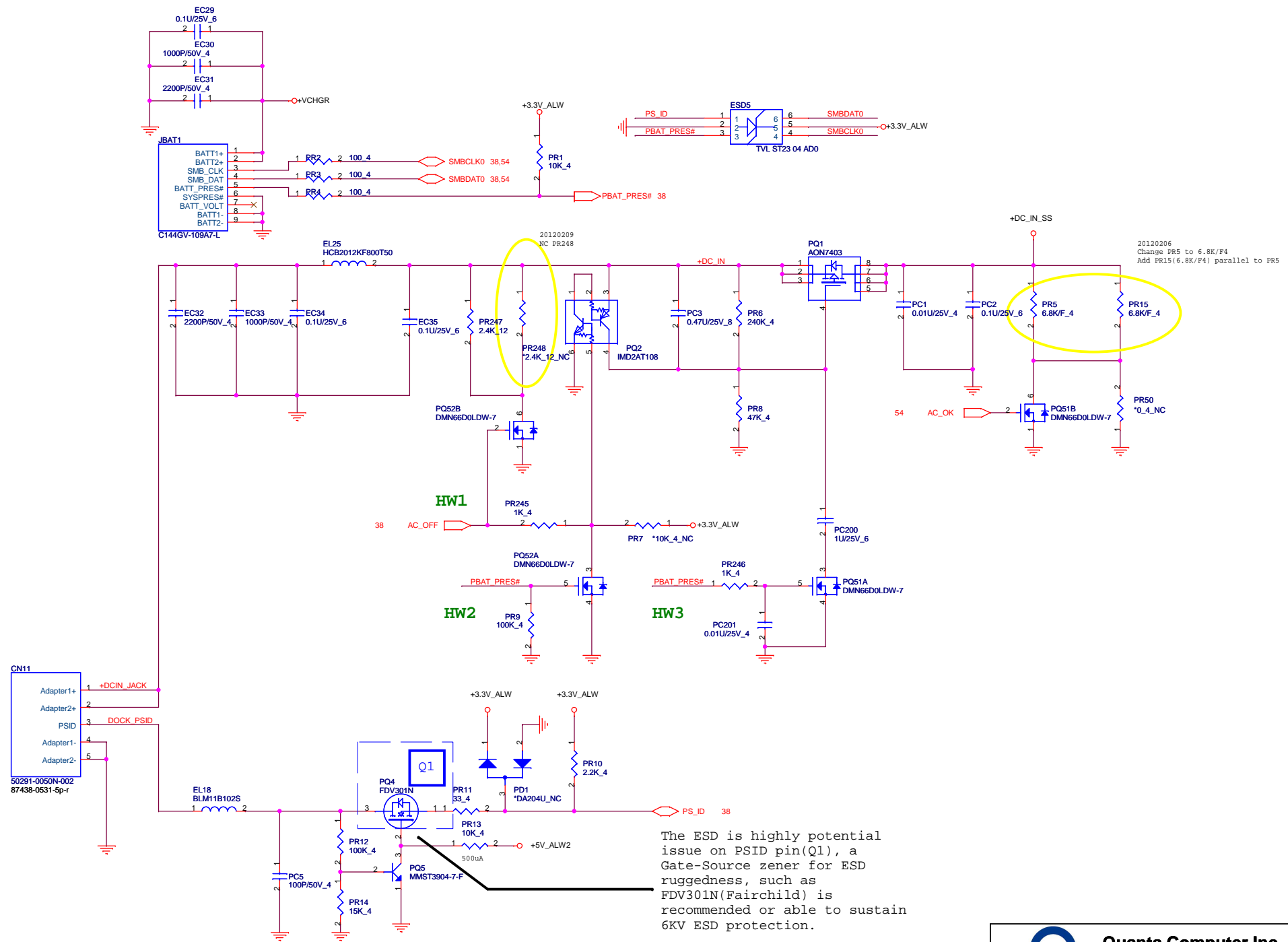
HDD activity LED.



Quanta Computer Inc.

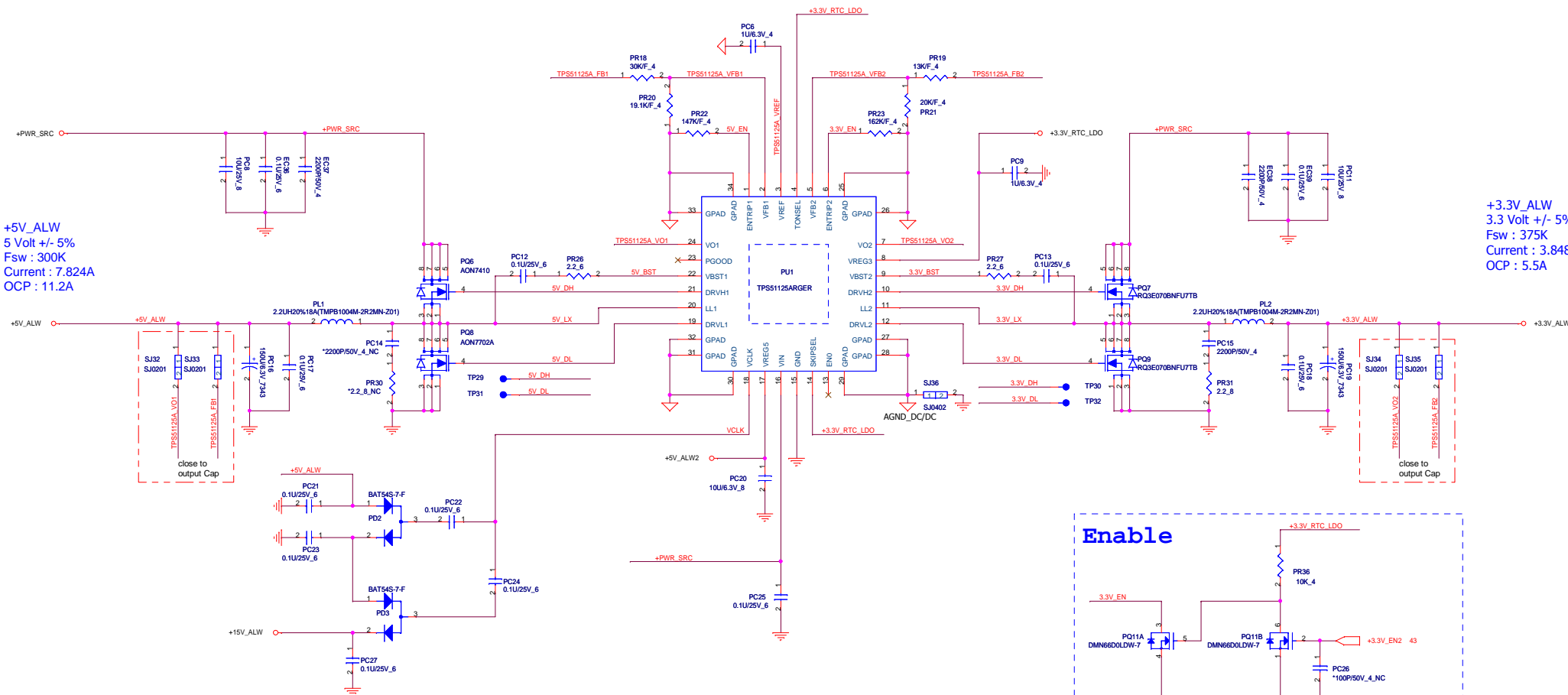
PROJECT : R08

Size	Document Number	Rev
	LED	1A
Date:	Monday, February 13, 2012	Sheet 45 of 55

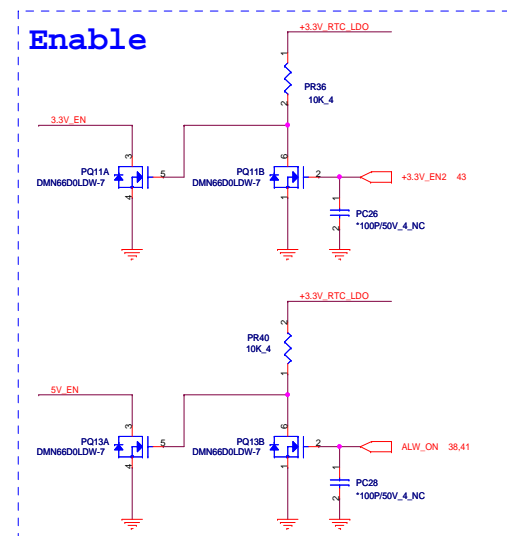


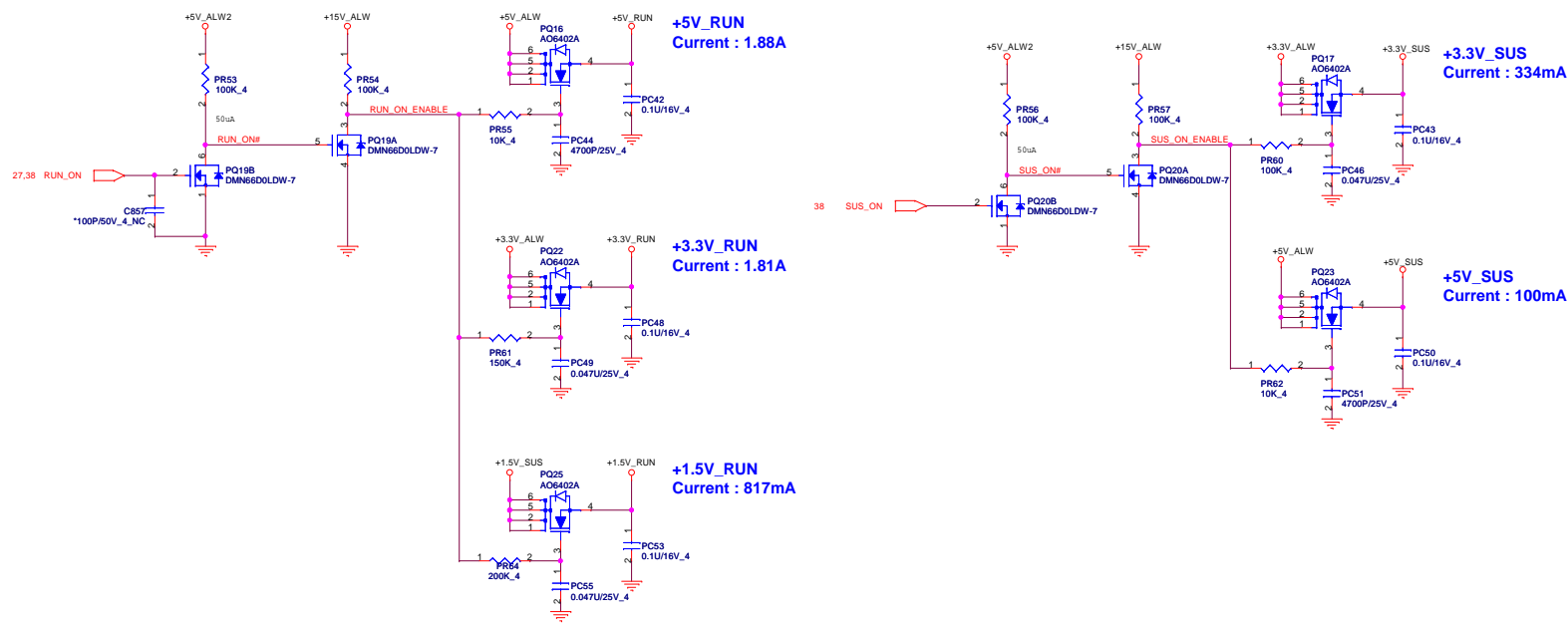
+5V_ALW
5 Volt +/- 5%
Fsw : 300K
Current : 7.824A
OCP : 11.2A

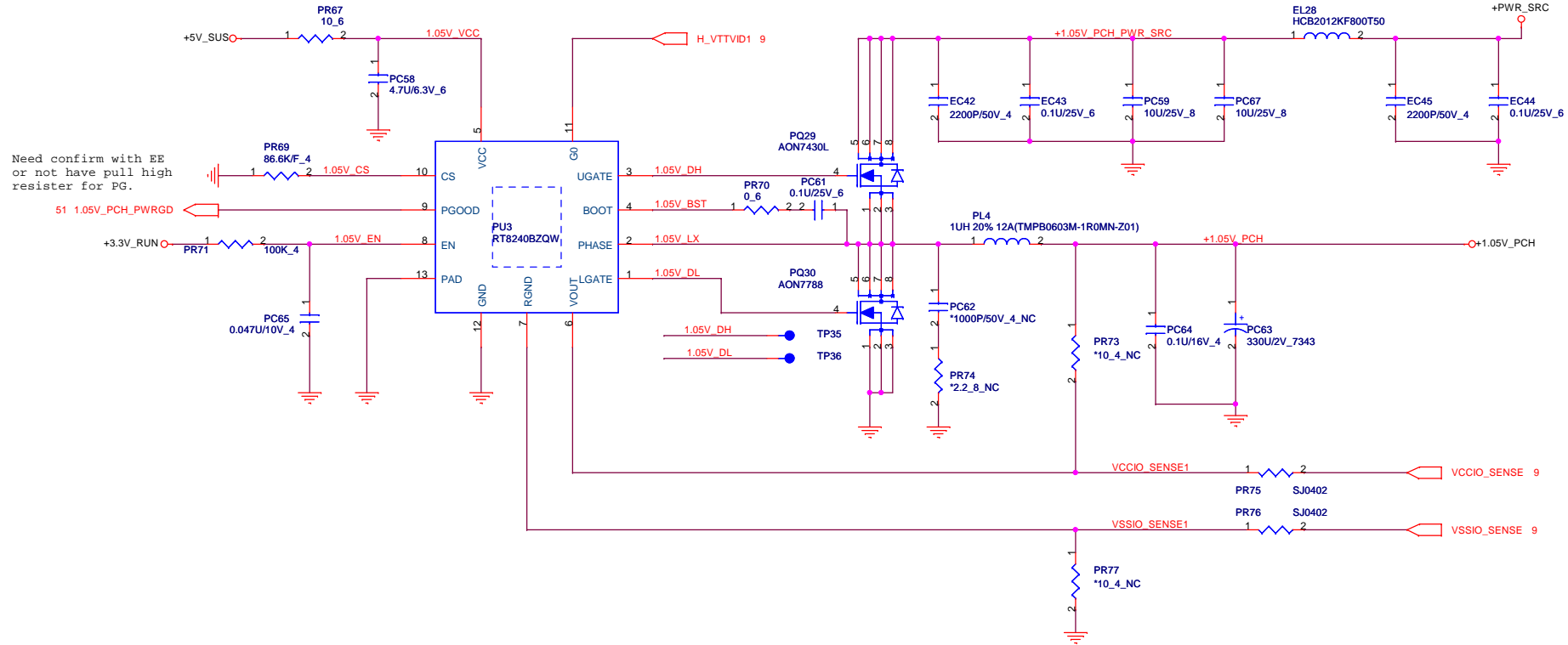
+3.3V_ALW
3.3 Volt +/- 5%
Fsw : 375K
Current : 3.848A
OCP : 5.5A



TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz







+1.05V_PCH
1.05 Volt DC +/- 2%
Fsw : 400K
TDC : 13.5A
OCP : 19.5A

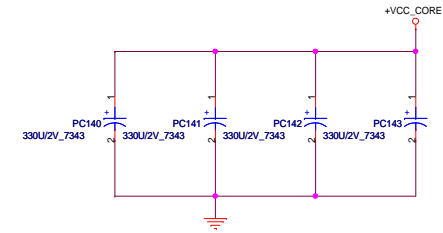
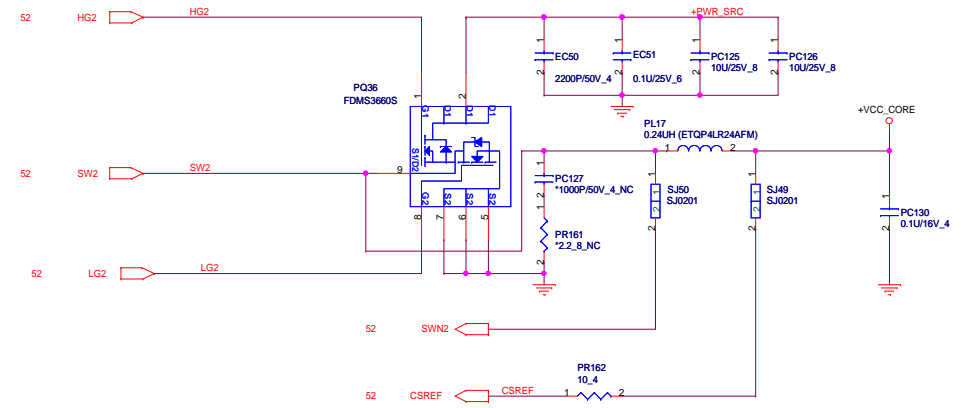
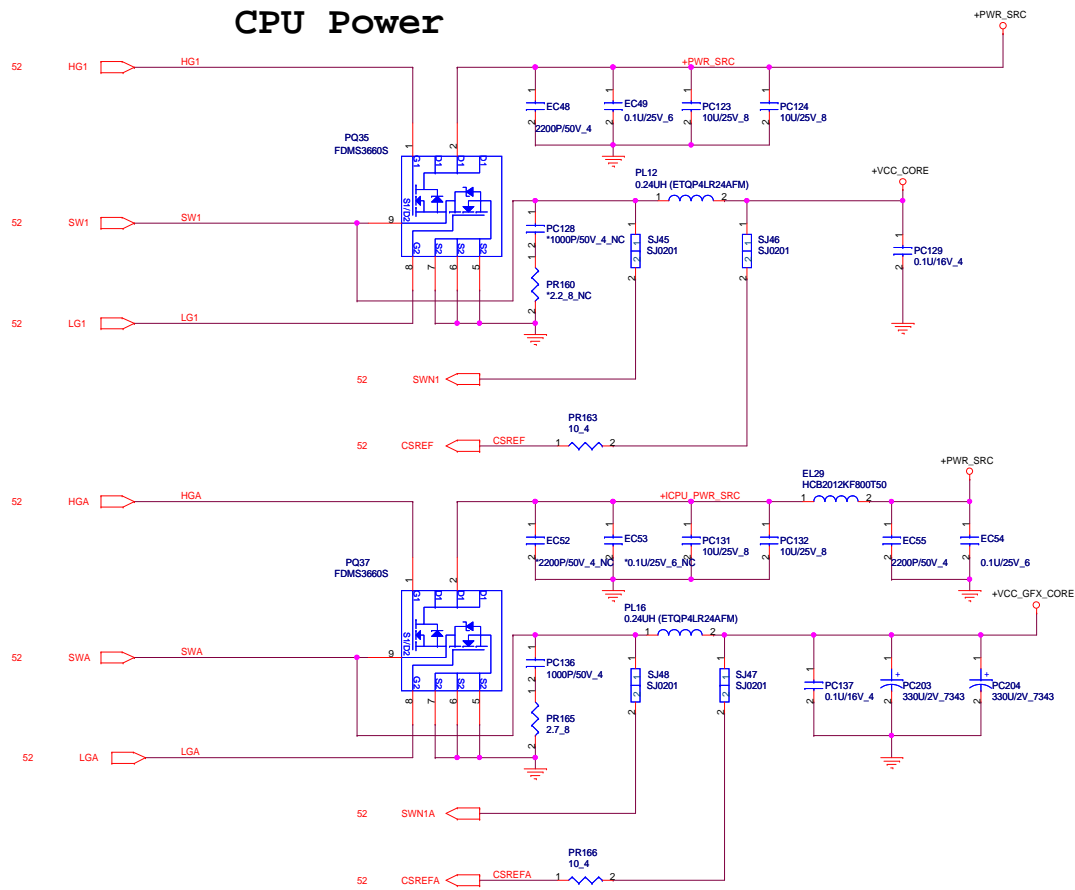


Quanta Computer Inc.

PROJECT : R08

Size	Document Number	Rev
	+1.05V_PCH / VTT (RT8240BGQW)	1A
Date:	Monday, February 13, 2012	Sheet 50 of 55

CPU Power



Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

